# Thermal avalanche in superconducting nanowire single photon detectors fabricated from WSi/aSi multilayers

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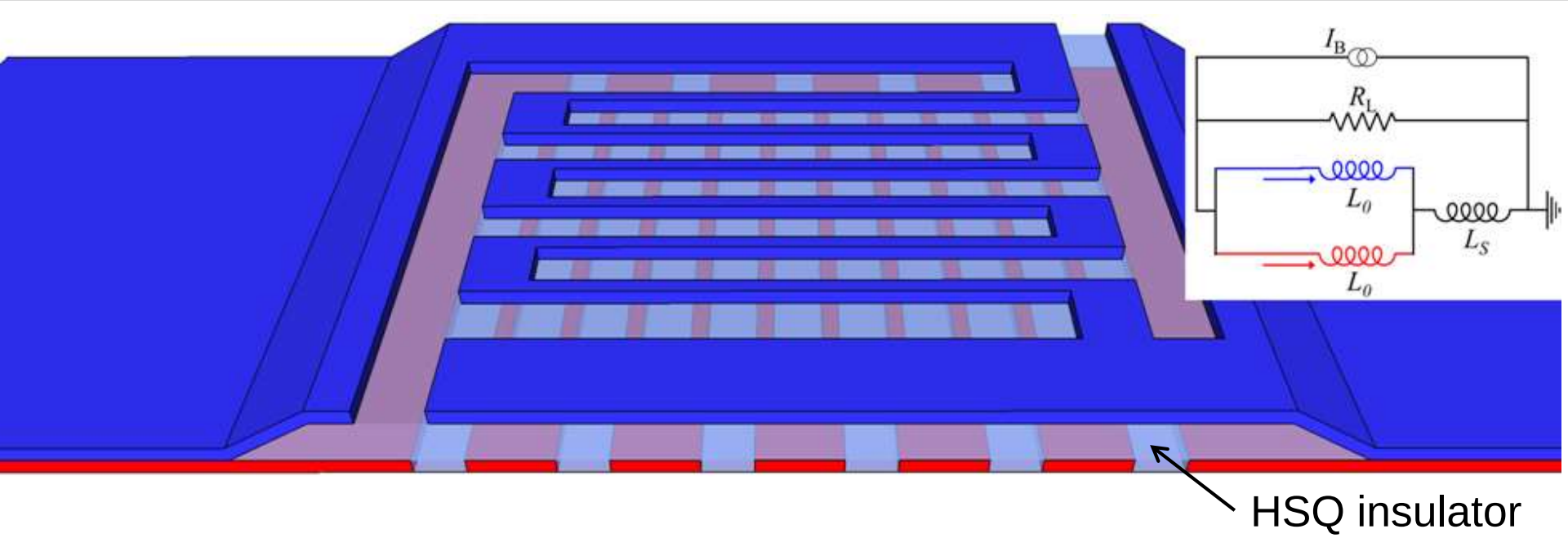
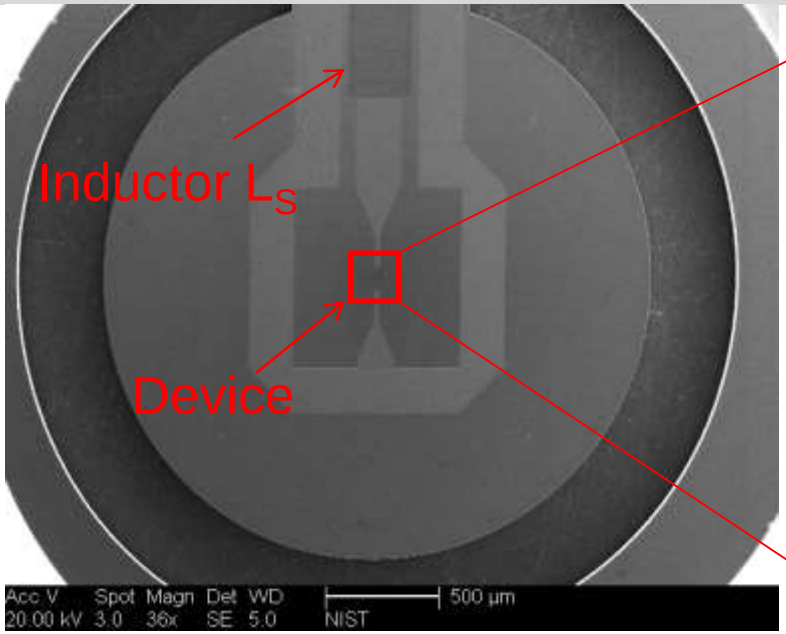
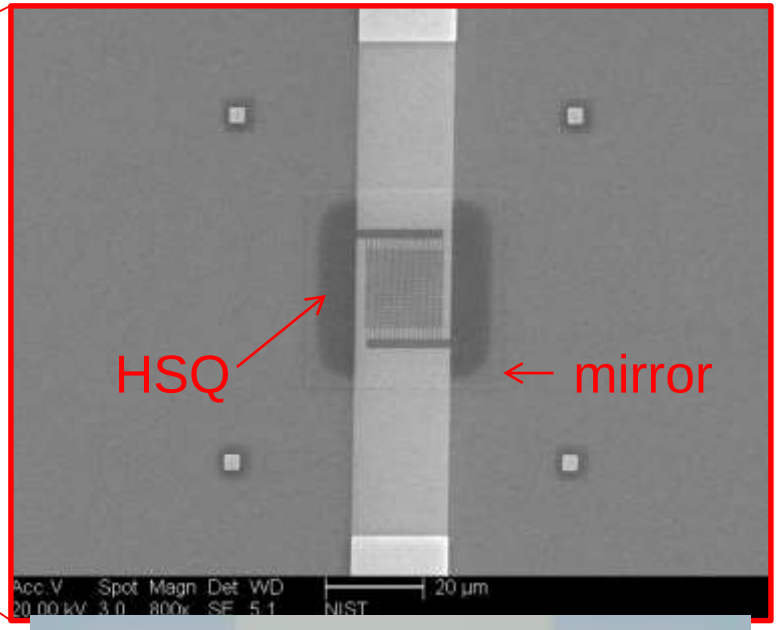
# Vertically-stacked WSi SNAP

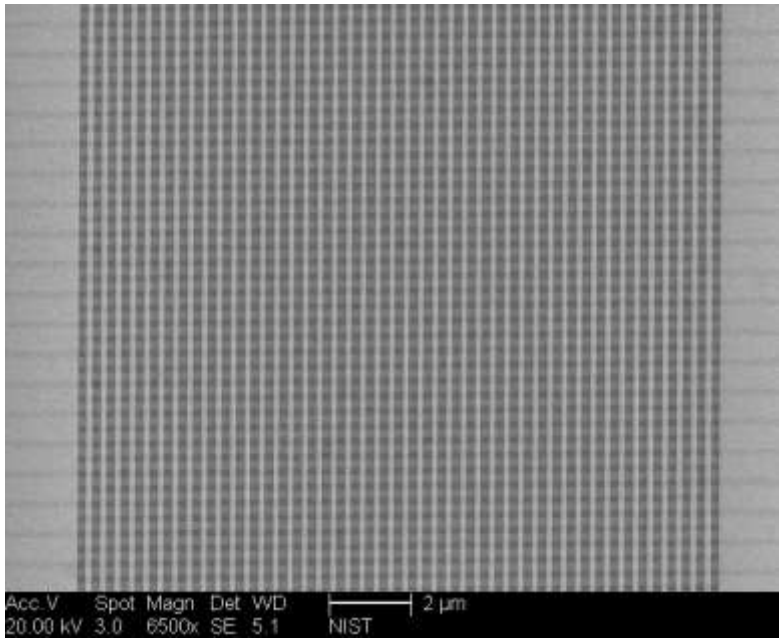


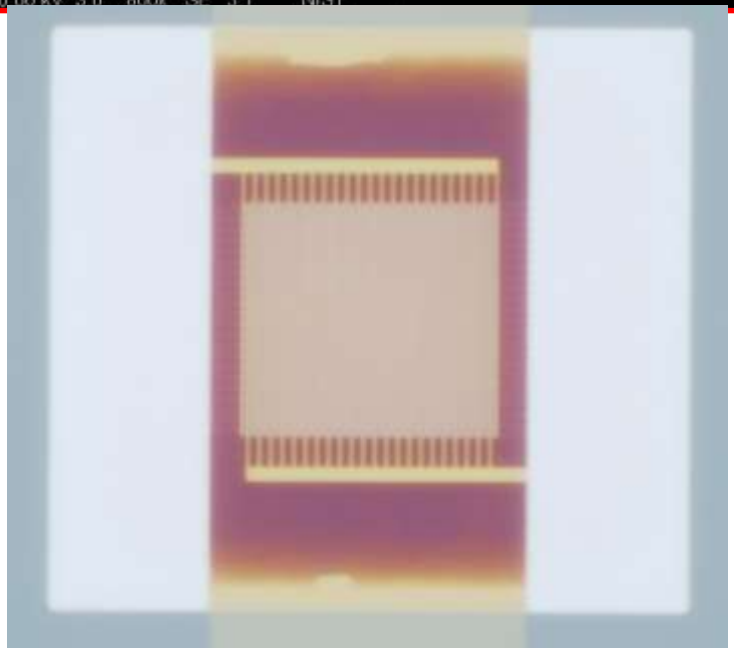

- Two SNSPDs stacked with orthogonal wire orientations, connected electrically in parallel (SNAP, superconducting nanowire avalanche photodetector)
- Orthogonal wire orientations eliminate polarization dependence
- Parallel bias scheme increases signal to noise ratio by factor of ~ 2
- Jitter ~ 500 ps due to large series inductor ($L_S$)

# Vertically-stacked WSi SNAP



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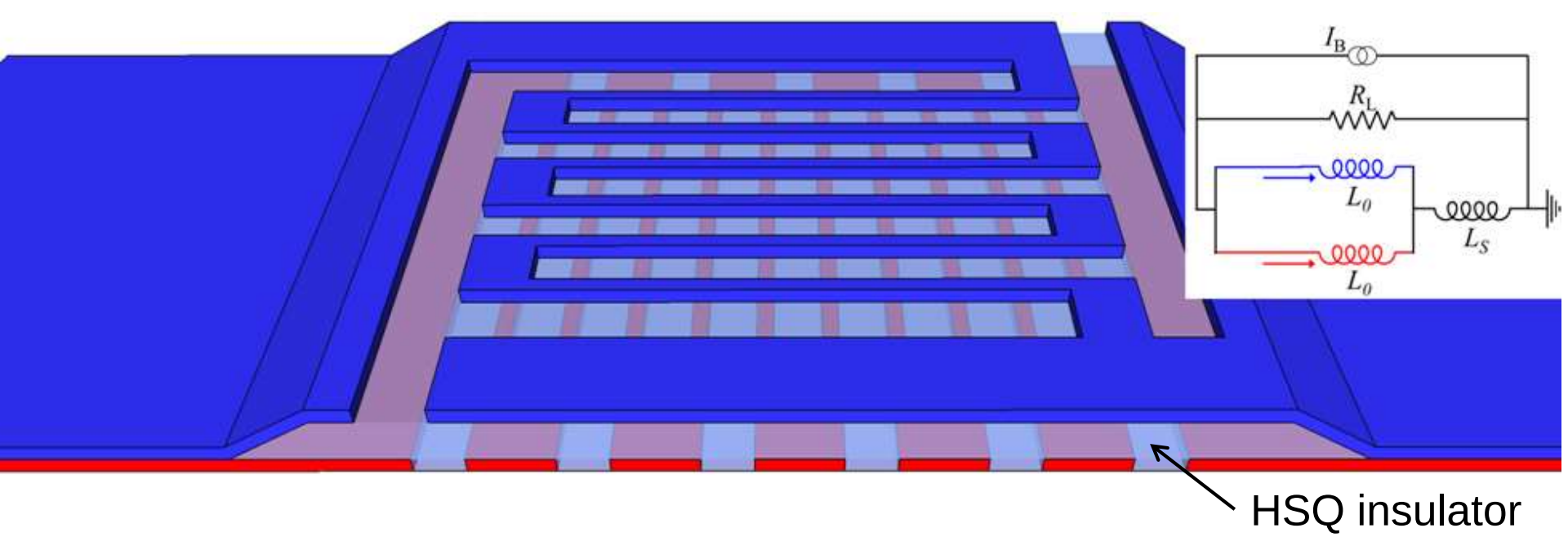
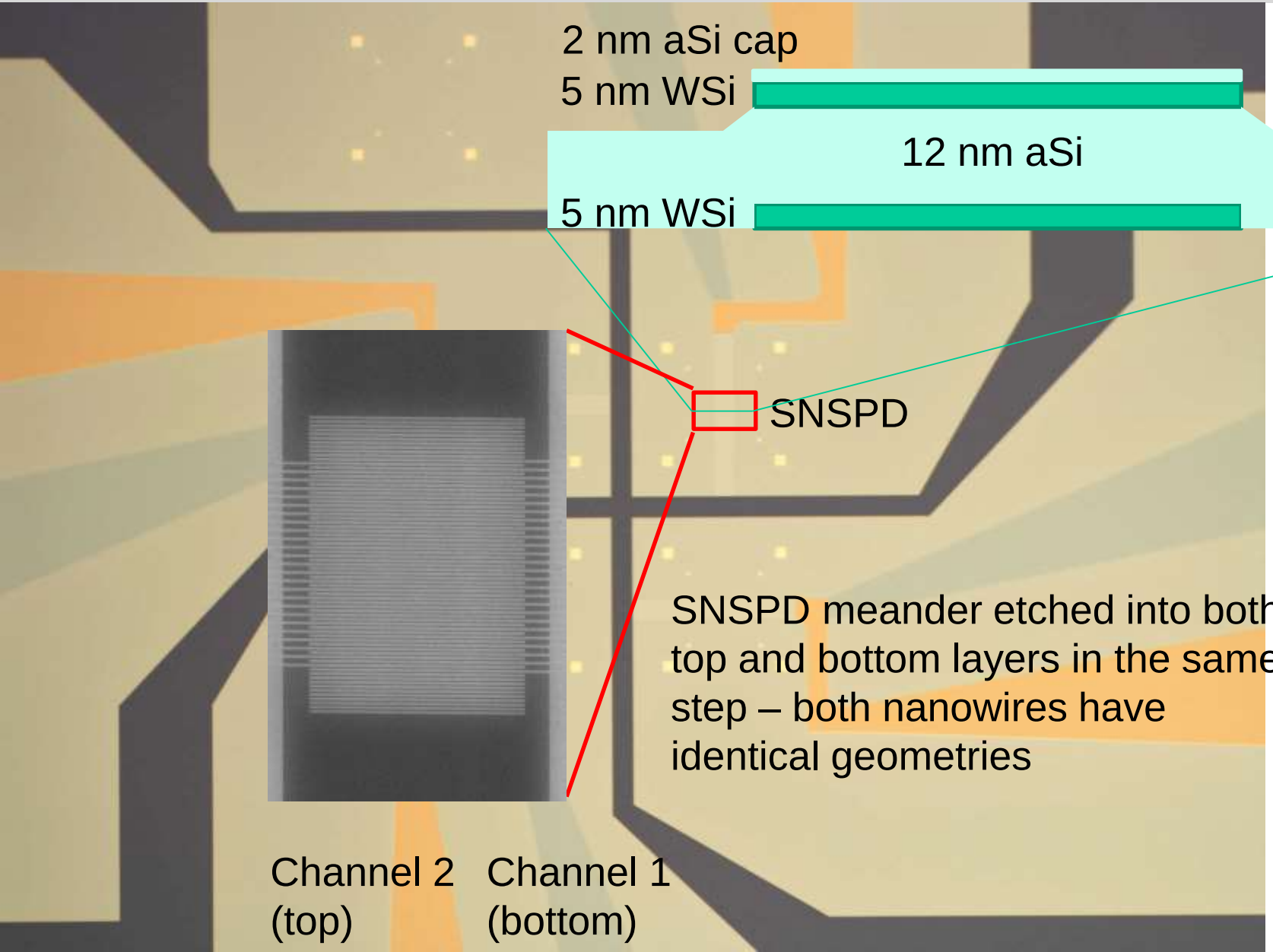


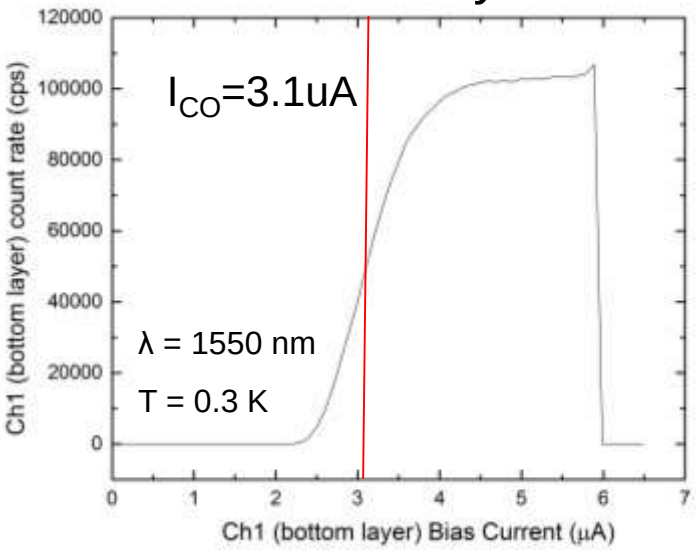

- In the detection process, a 0.8 eV photon (1550nm) becomes ~1 keV of energy due to Joule heating
- ~80-90% of this energy is lost to the substrate in the form of phonons
- If we could bias each layer independently, would we see detection events in one layer due to phonons emitted from the other?

# Fabrication of test device

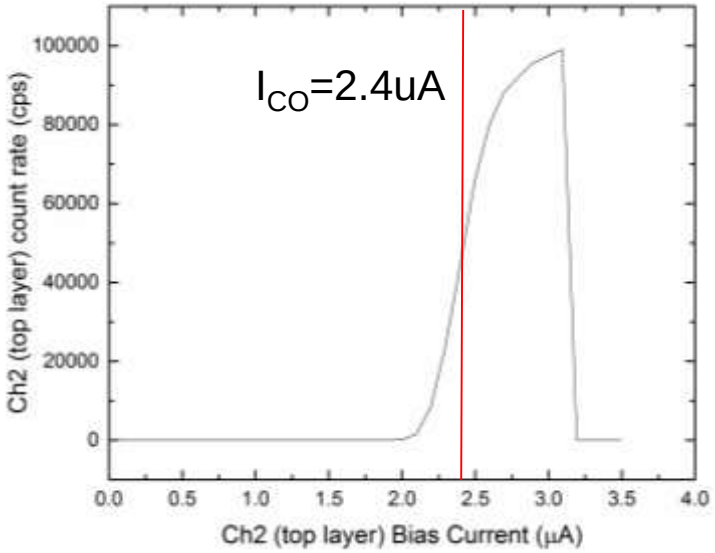


# Measurement Results

Bottom Layer

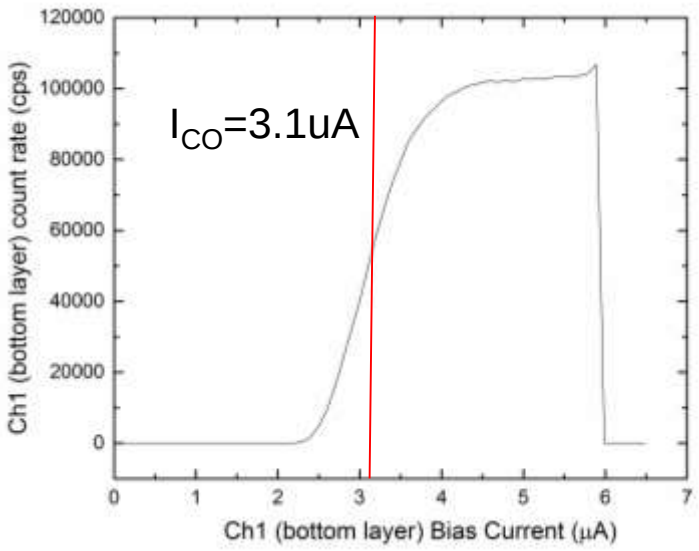


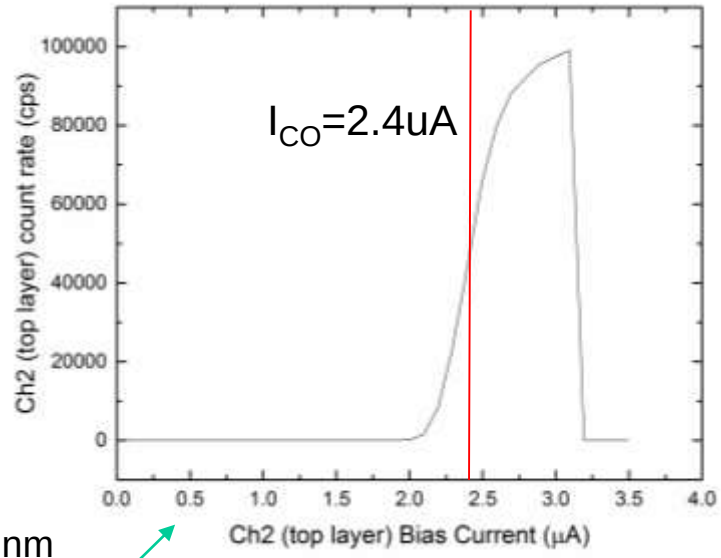

Top Layer

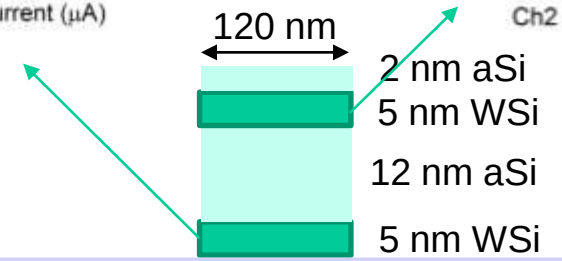



- Switching current ($I_{SW}$) of Ch2(top layer) is suppressed relative to bottom layer – possible contamination from processing of bottom layer
- Cutoff current ($I_{CO}$) is shifted to the left for the top layer, although both films have identical thickness and composition, nanowire geometries are identical
- Both layers are capped with amorphous silicon to prevent oxidation

# Measurement Results



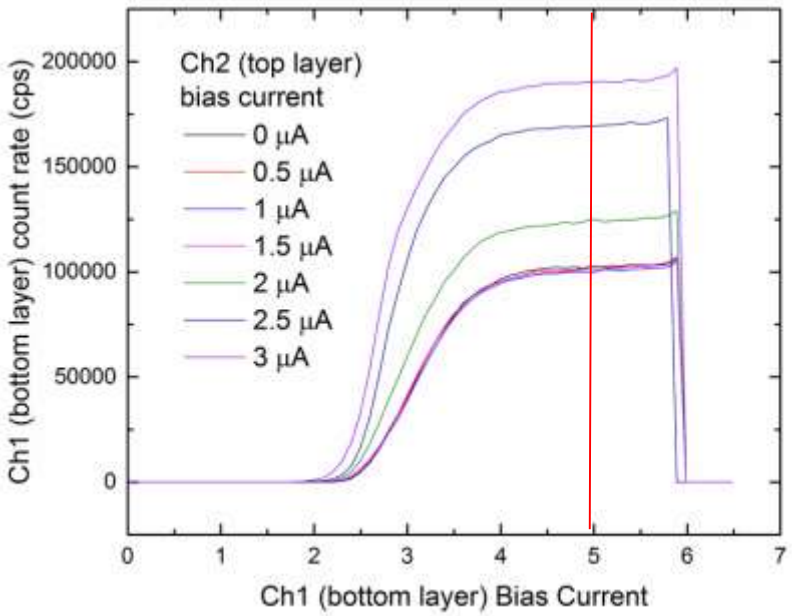




150 nm $SiO_2$

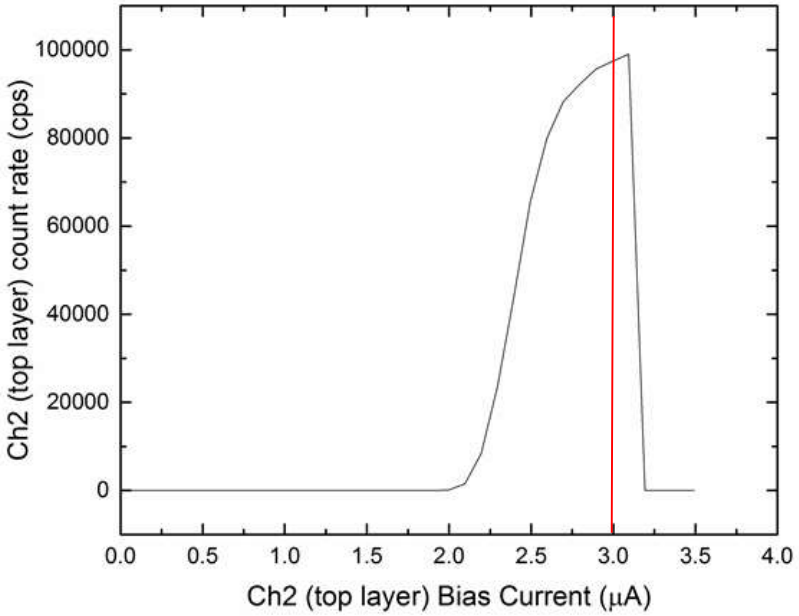
Silicon substrate

# Measurement Results

Bottom layer DE
varying top layer bias



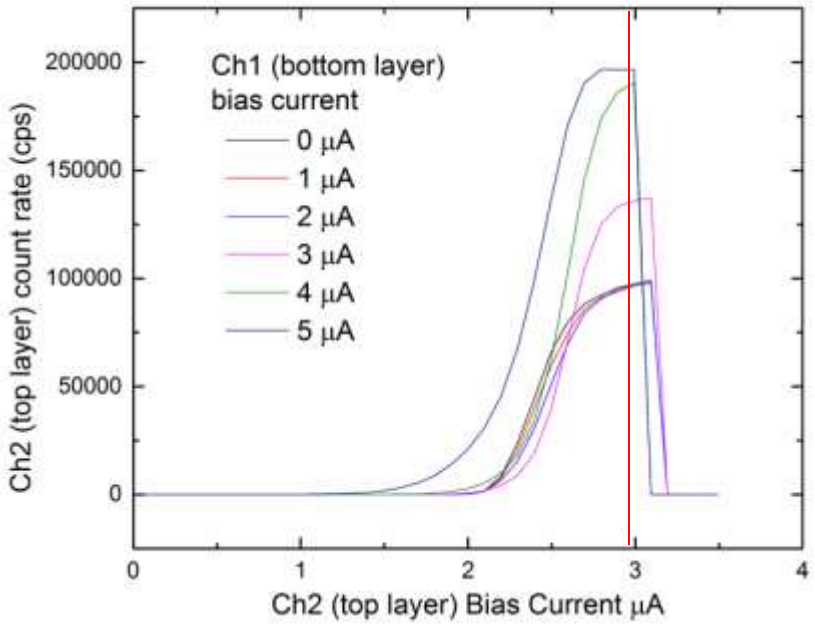

Top layer DE
Zero bottom layer bias



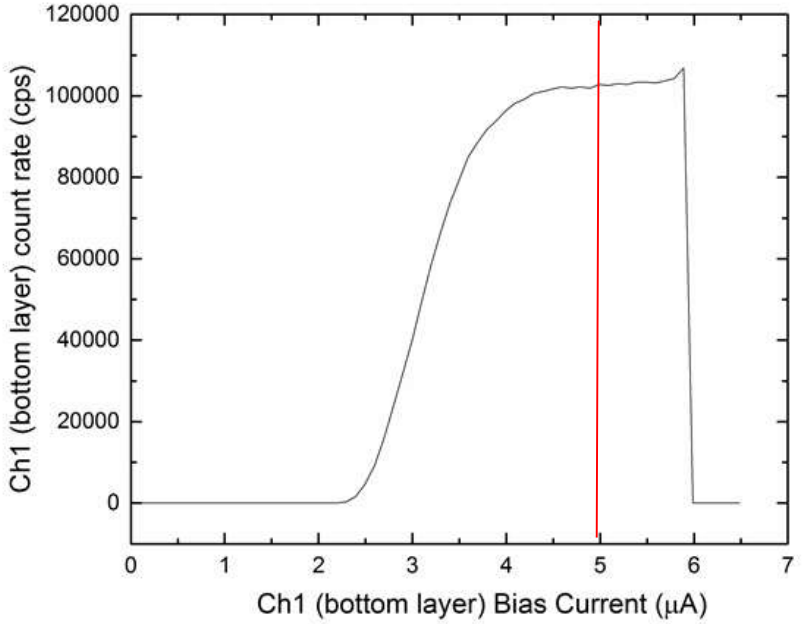

- Increase in count rate 87,620 cps
- At 3 uA bias, count rate of top layer is 97,420 cps
- 90% of pulses in the top layer result in corresponding pulses in the bottom layer

# Measurement Results

Top layer DE
varying bottom layer bias




Bottom layer DE
Zero top layer bias

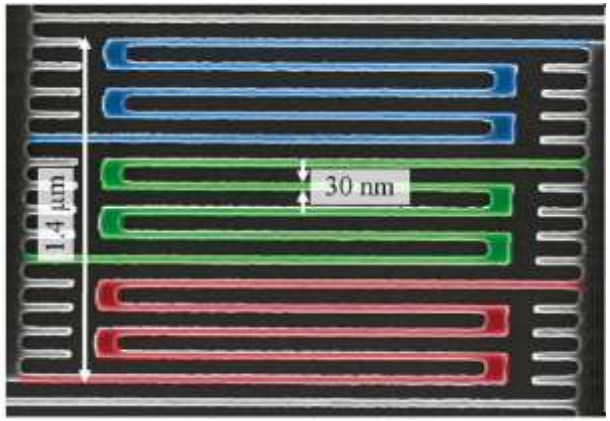


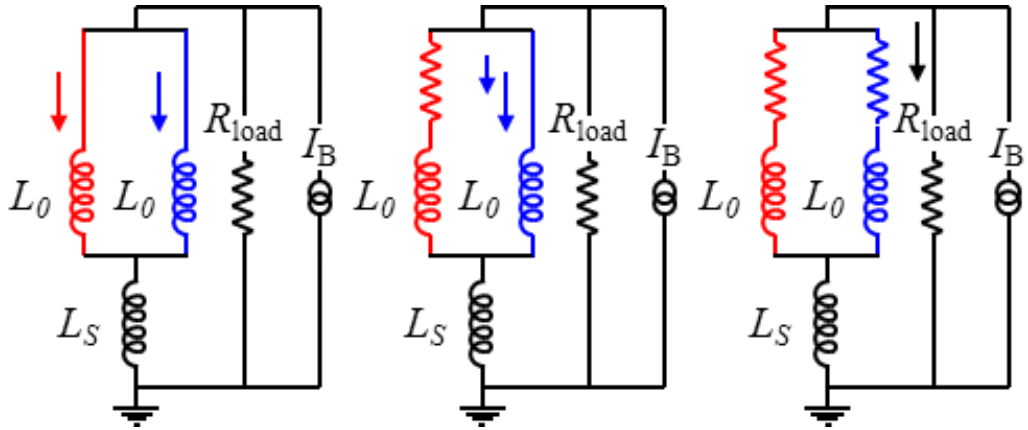

- Increase in count rate 99,180 cps
- At 5 uA bias, count rate of bottom layer is 102,780 cps
- 96.5% of pulses in the bottom layer result in corresponding pulses in the top layer

# Measurement Results

- 90% of pulses in the top layer result in corresponding pulses in the bottom layer
- 96.5% of pulses in the bottom layer result in corresponding pulses in the top layer
- Imbalance related to amount of Joule heating ($I^2R$) created in the detection process
- Bottom layer with 6 μA switching current can generate ~4 times the Joule heat of the top layer with 3 μA switching current.

# Superconducting Nanowire Avalanche Photodetector (SNAP)




F. Marsili, et. al., Single-photon detectors based on ultranarrow superconducting nanowires, Nano Letters **11**, 2048 (2011).

M. Ejrnaes, et. al., A cascade switching superconducting single photon detector, Appl. Phys. Lett. **91**, 262509 (2007).

- Parallel connection of N nanowires
- Can provide a photoresponse pulse with N-times-larger amplitude than an SNSPD
- Connected in series with an inductor $L_S=10L_0$ for N=2 in order for the avalanche to occur
- Large inductor $L_S$ significantly slows the rise time of the pulse
- Jitter proportional to slope of rising edge
- Pulse amplitude increases by 2x, but jitter degraded by $L_S$

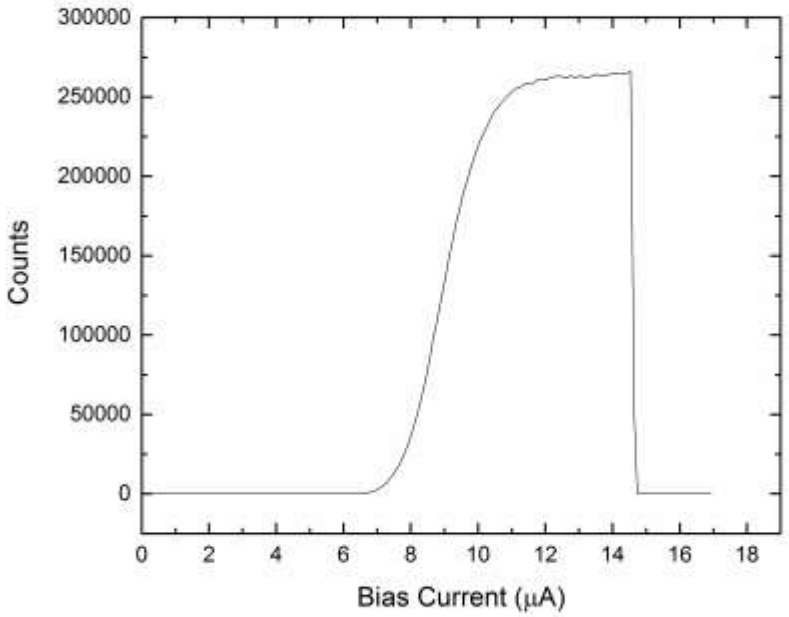
# Thermal SNAP

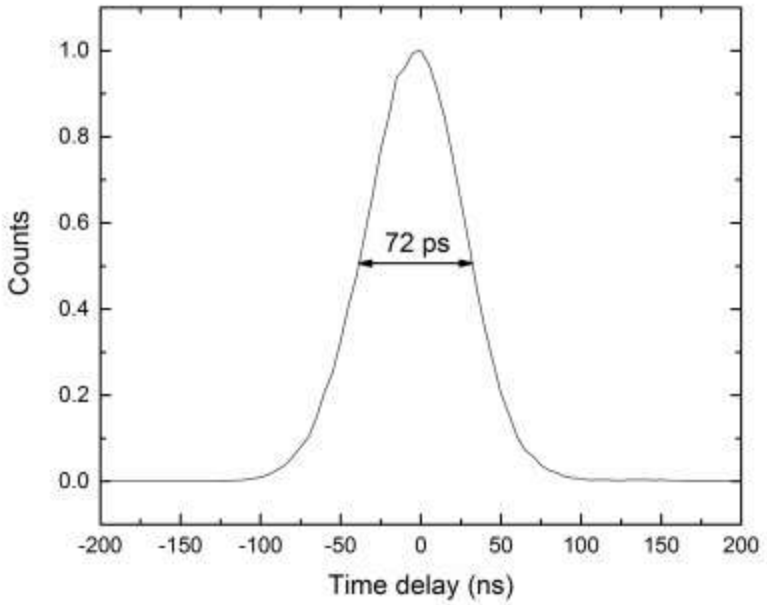
- Thermal interaction can be used to amplify signal from a single nanowire – thermal SNAP (superconducting nanowire avalanche photodetector)

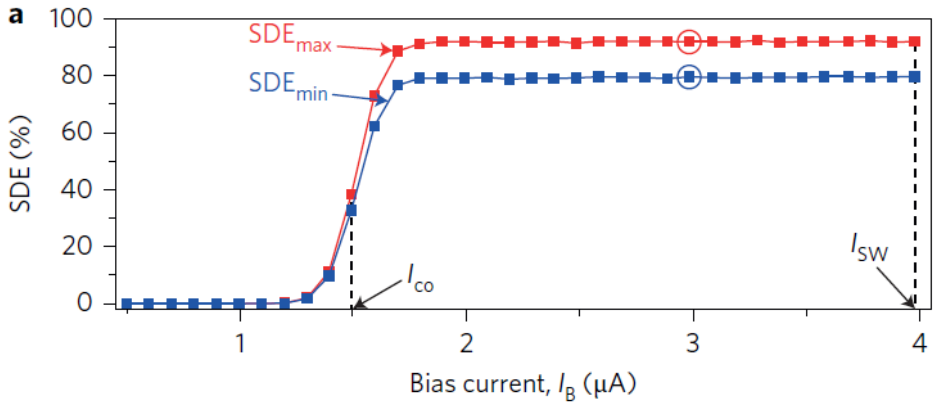
- Avalanche process is thermal instead of electrical
  - Instead of a redistribution of current causing the avalanche, it is caused by the thermal interaction
  - No extra inductance ($L_S$) needed!
  - slope of output pulse increases, jitter greatly improve

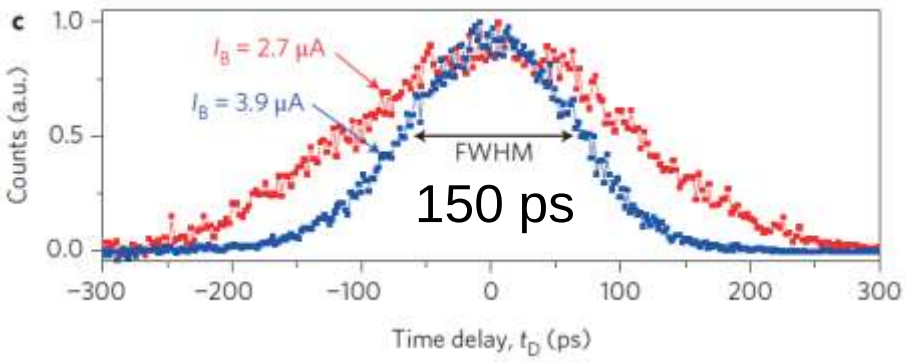
# Thermal SNAP

175 nm-wide nanowire, 4nm aSi




F. Marsili, et. al., Nature Photonics **7**, 210 (2013)

# Conclusions

- Stacked superconducting nanowires can exhibit strong thermal interactions

- Developed new device (TSNAP) based on superconductor/insulator multilayers
  - factor of 2 reduction in jitter compared to previous results
  - factor of 2 increase in absorption (simplifies fabrication of optical cavity, may allow the fabrication of ultra-broadband detectors)
  - factor of 2 decrease in kinetic inductance per square of material (enables larger area devices without degrading maximum count rate)

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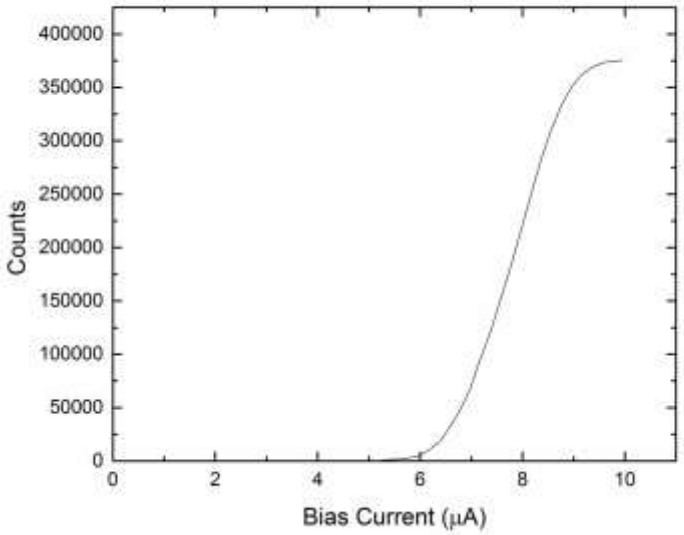
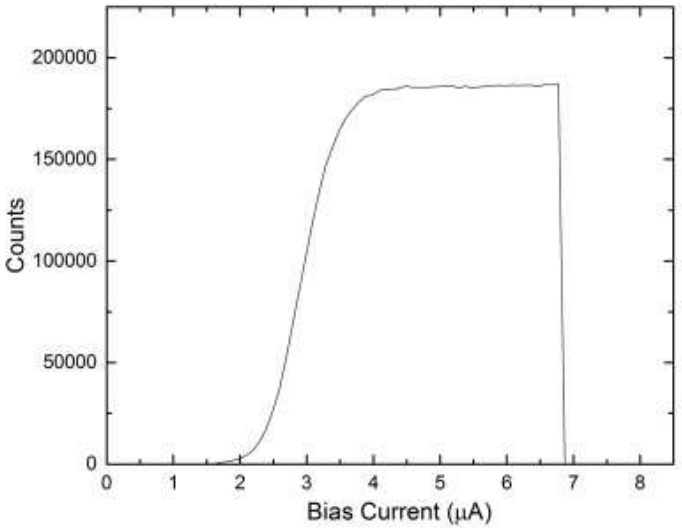
# Thermal SNAP

TSNAP 2nm aSi



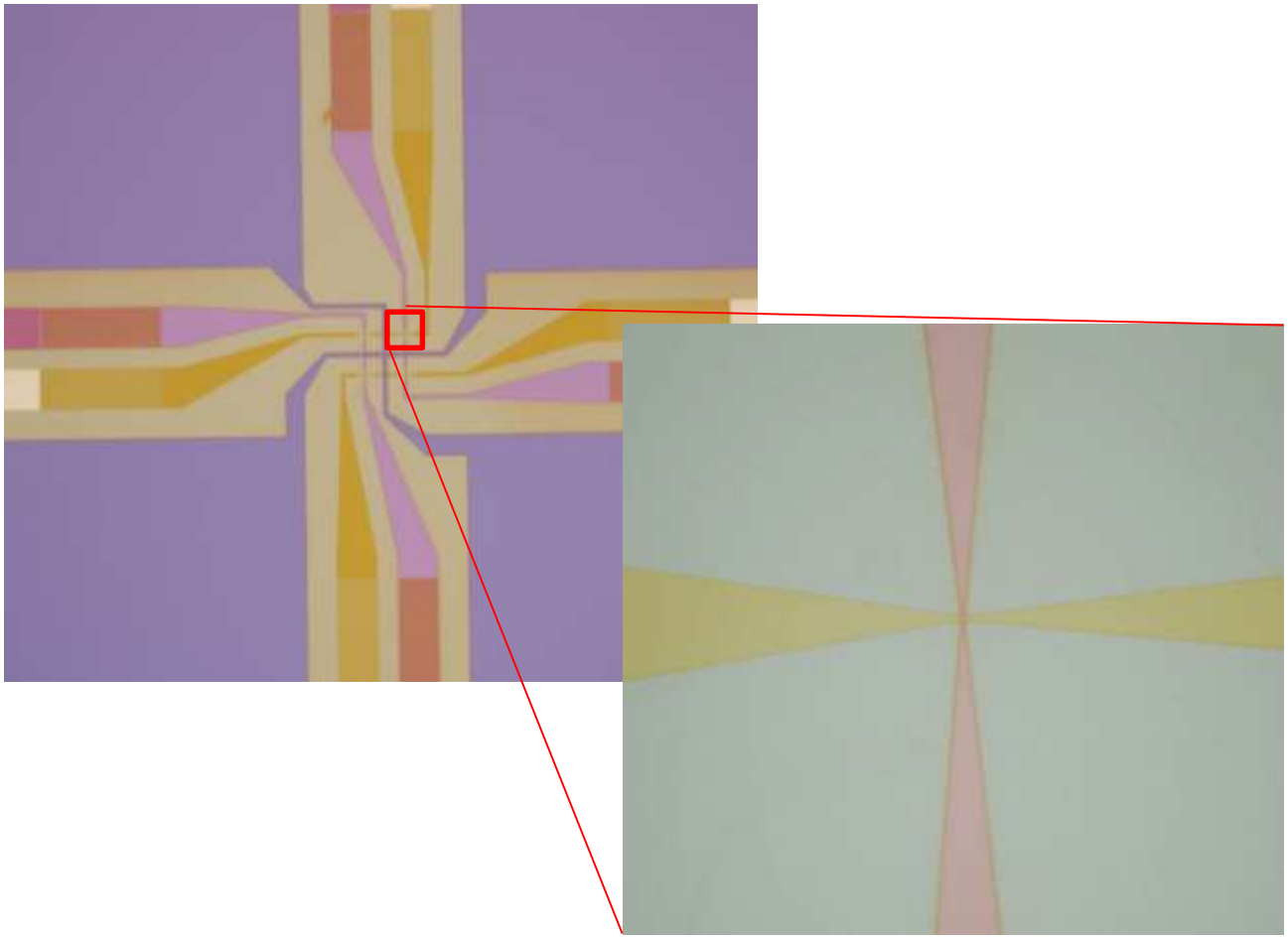

TSNAP 4nm aSi



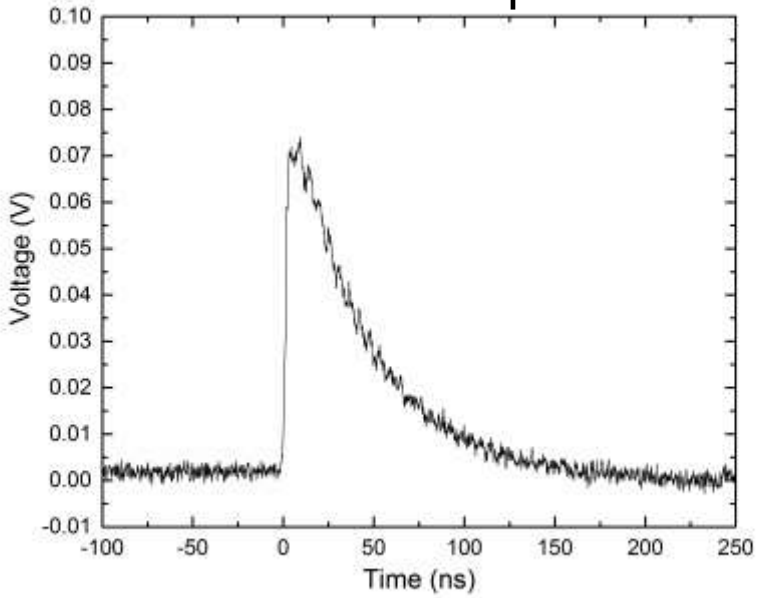

- 2 nm spacer not thick enough to adequately confine current to the superconducting layers, intermixing between layers likely
- 4 nm spacer thick enough, plateau significantly improved

# Conclusions

- Potential new class of superconducting logic based on thermal gating
  - build amplifiers and perform on-chip signal processing
  - similar to n-Tron except gate is electrically isolated from source/drain



Ch2 bias 3μA




Ch1 bias 0μA