Kintex-7 FPGA board for multiplexing and demultiplexing signals in a FDM readout for superconducting mm-wavelength detectors

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We present the hardware and software process to implement an algorithm on a Kintex-7 FPGA board for multiplexing and de-multiplexing bias signals for superconducting mm-wavelength detector arrays operating at sub-Kelvin temperatures. The process of programming the board using Vivado and Xilinx ISE is explained. In order to test the performance of this method, an 8-channel resonator circuit at 4 K is fed with a multi-tone signal (0.3-1 MHz) and measured by a SQUID in a TES scheme read out. The algorithm and set up for preliminary tests and debugging are presented as well as some current results.

Vivado and Matlab programming

Design and co-simulation of signal generation and demodulation.
Matlab + Simulink + System Generator + HDL Coder

Programming FPGA. Vivado: I/O pin assignment, Synthesis, bit files, etc.

Main modules in VHDL code

Clock (245MHz)

Demodulation

Modulated signal 14 bits

Modulated signal

SFR control

DDS

Bias signal 18 bits

DAC280 800 MSPS

Bias signal

Nuller

ADS6249 250MSPS

FMC150 Card

To PC

Conclusion and Future work.

We are using Simulink and Vivado for programming a FPGA board for a FDM scheme with good results so far. The inherent complexity of FPGA projects usually implies the participation of a experienced team in digital systems. Nevertheless, the labor of programming could be greatly simplified by using tools for planning and testing each stage of the work before make the actual code in VHDL. This also could save time in the whole process but specially during debugging the code. The next step in our project is to finish tests using the SQUID and the resonator circuit before continue with the design of an integrated circuit with real detectors.

References.
