A demonstration of cryogenic trans-impedance amplifier using fully-depleted silicon-on-insulator CMOS operational amplifier for far-infrared image sensor

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Abstract

We are developing a low power cryogenic readout integrated circuit (ROIC) for large format far-infrared image sensor. As cryogenic electronics, we use fully-depleted silicon-on-insulator (FD-SOI) CMOS technology. FD-SOI MOSFETs show very stable static characteristics at 4.2 K. We report the trans-impedance amplifier (TIA) circuit using FD-SOI CMOS OPAMP at cryogenic temperatures. In order to evaluate performance in measuring current for the TIA circuit, we combined the TIA circuit with the germanium blocked impurity band (Ge-BIB) detector as very small and calibrated current source.

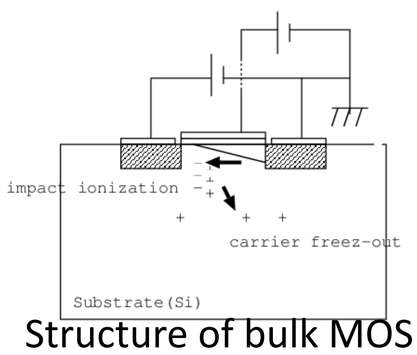
Introduction

- Our goal is large format far-infrared image sensors
  Ge-BIB detectors + cryogenic electronics
  (See Hanaoka-san's poster and Wada-san's poster)

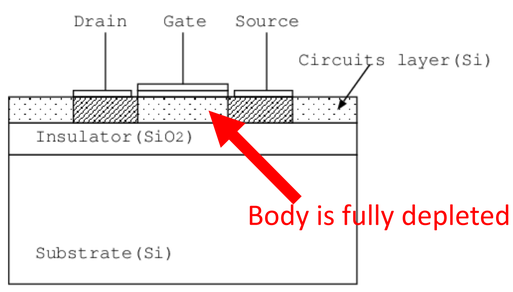
- Ge detector must be cooled down under 2K.
- Conventional bulk CMOS shows anomalous behavior at cryogenic temperatures
  - carrier freeze out
  - impact ionization

  ⇒ Potential of FET body becomes unstable

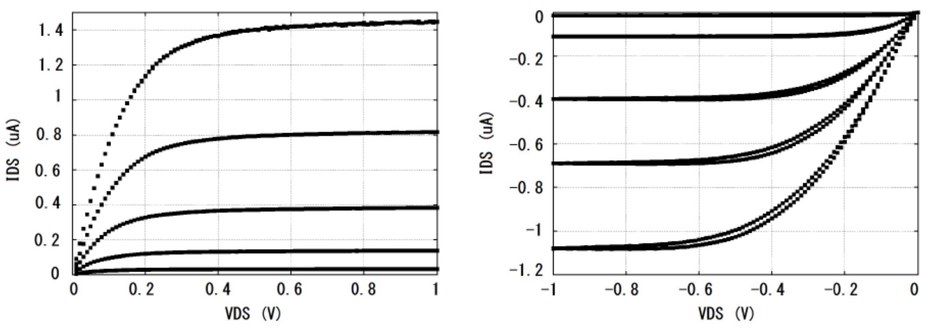
- Fully-depleted SOI CMOS shows very stable static characteristics under 4 K.



Structure of bulk MOSFET



Structure of FD-SOI MOSFET



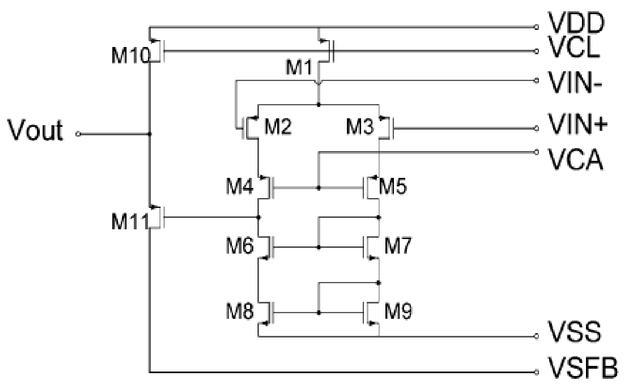
I-V curves of the FD-SOI MOSFETs
L:NMOS Vg=0.9 V⇔1.1 V
R:PMOS Vg=-1.65 V⇔-1.25 V

Cryogenic readout electronics using FD-SOI CMOS

- We successfully developed a cryogenic operational amplifier (OPAMP).

- We will design TIAs and CTIAs for measurements of ultra-low current (～ fA).

- Low power consumption
  - large format
    a few mW for 32×32 pixels (1uW/pix)
  - low background
    no need to warm up
- High gain
  suitable for feedback circuits



Circuit diagram of our OPAMP

Performance of the FD-SOI CMOS amplifier at 4.2 K

	design	measurement
Open loop gain	>1000	>7000
Power consumption	1.1 μW	1.3 μW
Output Voltage swing	>1V	1.3 V
Input referred noise at 1 Hz	14-20 $\mu V/\sqrt{Hz}$	19 $\mu V/\sqrt{Hz}$
Input offset voltage	0 mV	2mV
Variation of input offset voltage	0 mV	4.2 mV(1σ)

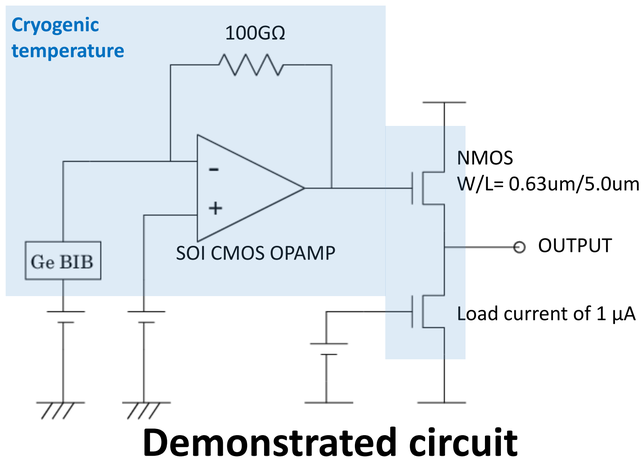
H. Nagata et al. IEICE Trans. Commun. Vol.E94-B, 2952, (2011)
T. Wada et al. J Low Temp Phys 167:602-608 (2012)

A demonstration of trans-impedance amplifier

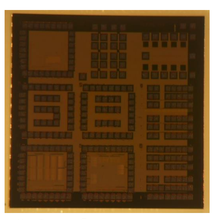
Goals
- Operation under 4 K.
- Measurement of ultra-low current(fA)

- Ge-BIB detector as very low and calibrated current source.
  an intrinsic Ge + a Ge doped Ga of 1E+16/cc
  H. Kaneda et al.,
  JJAP 50, 066503 (2011)

We measured dark current of Ge-BIB by using FD-SOI OPAMP at cryogenic temperatures.

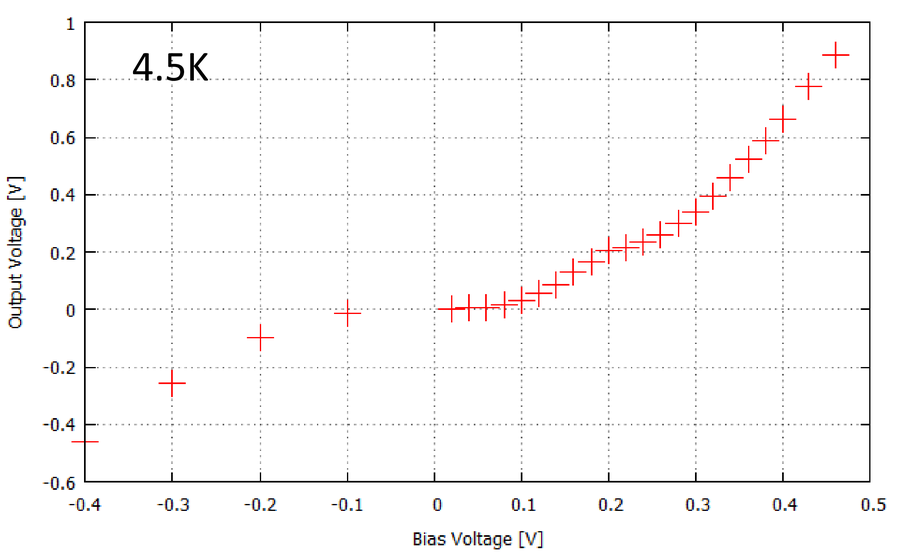


Demonstrated circuit



Test chip (2.9mm×2.9mm)
There is an OPAMP in this chip

Result



Output 32mV@Bias 0.1V ～300fA

Next step

We will measure dark current 1fA at 1.8 K.
In addition, We will evaluate the image sensor of 5×5 pixels.