The test board, with 3 ASICs:

- Functions repetition in ASICs:
  - Circuit CryoCan1: one of the 4 channels analog (left) and digital (right)
  - Circuit CryoCan2: 17 other inputs
  - Circuit CryoCan3: digital input
  - Circuit CryoCan4: digital output

- Optimization of the implementation:
  - Mechanic, printed circuit and integrated circuits have been developed together to try to optimize the design and fit with the very high integration level (24 ASICs in 23 x 16 mm) on one-layer PCB.
  - This appears in the ASIC pin-out and in the circuit dimensions and shape (same width as HEMT strips).

- Tests at 4 K:
  - The test board, with 3 ASICs:
    - 8×8 ASICs (CryoCan1, CryoCan2, CryoCan3)
    - Implantation area: circuits by bonding
  - Two test benches have been developed for test at 4 K:
    - One using a liquid helium tank for test of the electronics alone.
    - The other using a cryo-cooler for test with the electronics connected to a detector at 50 K.

Our technical solution:

- Two electronics stages:
  - 1) Input stage in HEMT transistors: gain> voltage amplifier
  - 2) Follow-up stages in SiGe/CMOS: equalizing and amplifying ( bipolar for analogic, CMOS for digital)

- Input stage is powered only when read:
  - To avoid detector perturbation when input stage is commuted.

Architecture:

- A power supply adjustment system that allows to adjust channel by channel the input stage polarization to the threshold voltage of the transistor.
- A passive or active compensation circuit to increase, if needed, the bandwidth at constant detector resistance.
- A test system, that allows to transmit to the acquisition system and at long distance, using the output signal cables (coaxial), the internal signals, power supplies and reference voltages, for control.
- A serial link protocol, that is used to configure the circuits and adjust the DACs, and includes a physical circuit address, allowing to place many circuits on a unique bus, and to address them individually.
- A radiation hardness reinforced by the duplication of every latches, to detect and signature SEU.

The electronics needed:

- Electronics as close as possible to the cold detector in works at low temperature: 2.5 K to 15 K
- Functions: amplification/amplification amplification, 4096 input channels.
- Should fulfill 4 main constraints:
  - Very high input impedance (>10 MΩ) to fit to the high impedance of the detector (1 MΩ)
  - Bandwidth > 10 kHz with 1 MΩ detector
  - Input capacitance > 5 pF not to slow down the signal.
  - Ultra low noise (<1 nV/Hz @ 1 MHz)
- Very low dissipation: <1 mW per output signal, which gathers 32 multiplexed input signals, to heat as less as possible the cryo-cooler.
- Main difficulty: the 3 last constraints (bandwidth, noise, dissipation) are antagonistic.

Use of two technologies of cryo-compatible transistors:

- HEMT transistors developed by LPN
  - Advantages: very high input impedance
  - Disadvantages: increasing of noise at low frequency
  - ... but LPN has acquired great performances, and improve them even more.
- SiGe/CMMOS technology by AMS
  - Advantages: commercial technology, complex circuits possible
  - Disadvantages: very expensive.

Multiplexing and amplification functions split into two ASICs, located at 2 temperatures (~2.5 K and ~15 K), to optimize the power load on cryo-cooler.

A full scale electronics, ideal to read 4000 channels:

- 34 input channels (33 Qab + 1 reference + 1 thermic control), followed by a 34 to 1 multiplexing
- Each input can be include or exclude of the inputs scan
- Commutation frequency: 1 MHz
- For each channel: 1 measurement every 34 µs
- Integration of 6 bits low consumption DACs to:
  - Adjust the anti-charge injection system (to avoid detector perturbation when commutation).
  - Adjust a baseline equalization system, that decreases the amplitude of the frame formed, at the multiplexed output, by the successive channel base levels, in order to increase the useful dynamic and decrease the over-dissipation induced by this frame.