

A 1: 128 multiplexing rate Time Domain SQUID Multiplexer

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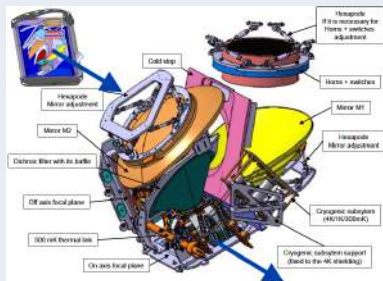


Low Temperature Detectors - LTD16
20 - 24 July 2015 - Grenoble

Q & U Bolometric Interferometer for Cosmology - QUBIC

Cosmology experiment for B-mode polarization of the Cosmic Microwave Background

Bolometric Fizeau interferometer

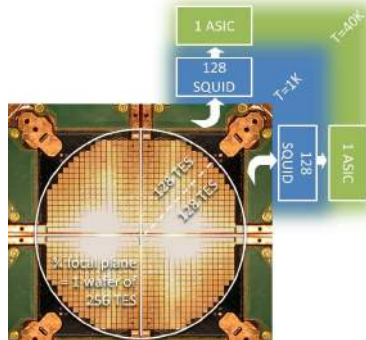


- 45cm window / 14° field-of-view
- 400 back/back horn (looking sky)
- 400 switches (self calibration)
- Off-axis Gregorian (combiner)
- 2 × 1024 filled array (150/220GHz)

A. Tartari *QUBIC: A Fizeau interferometer for B-Modes*
Thursday 23 - Session 5

NbSi TES focal plane imager

- Interference fringes (synthesized image)
- 1024 NbSi TES on 4 wafers (×2 freq.)
C. Perbost *A 248 TES Array for CMB B-mode detection* Poster



Present work, sub-system :

256 TESs, 256 SQUIDS (TDM), 2 ASICs (LNA + bias)



Outline

- 1 : 128 TDM multiplexer topology
- 2 Readout chain
 - SQUID stage
 - Cryogenic integrated circuit
- 3 Multiplexed signal, FLL and demultiplexing

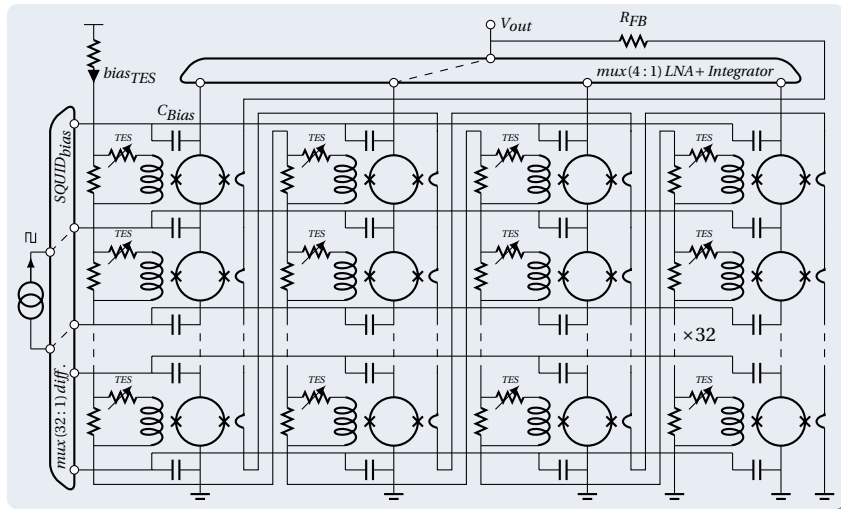


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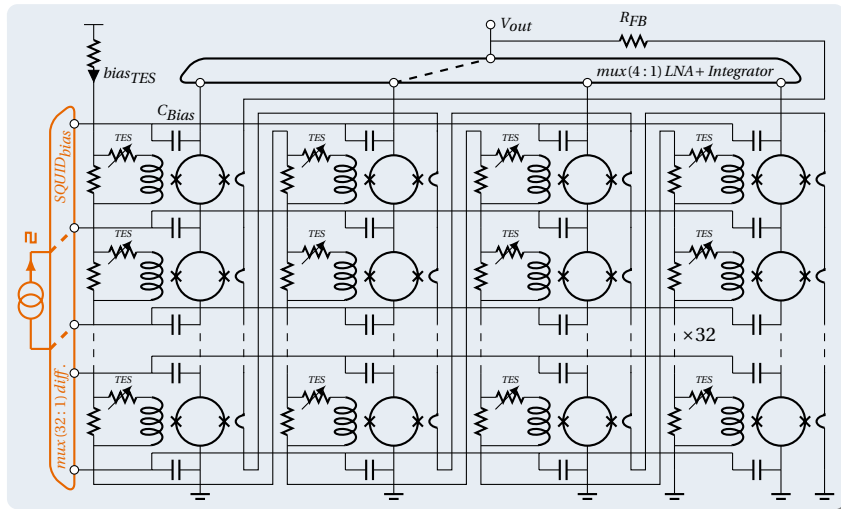
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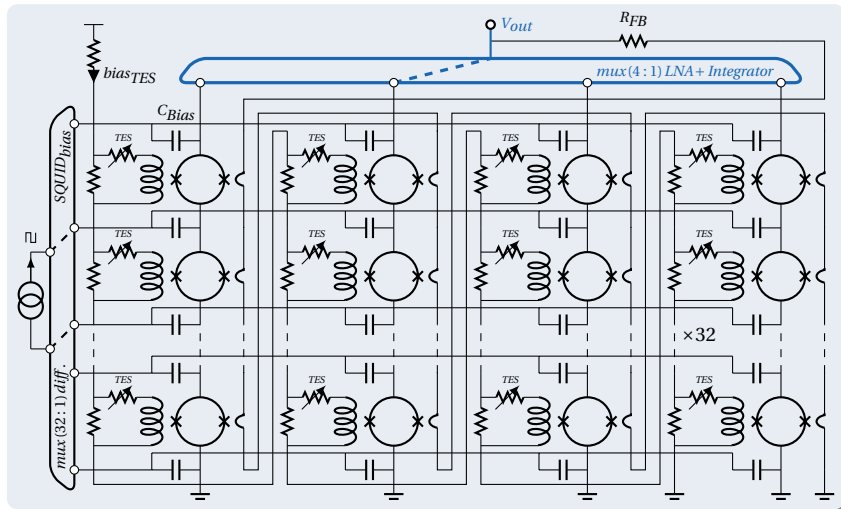
TES readout topology based on 2D multiplexing scheme



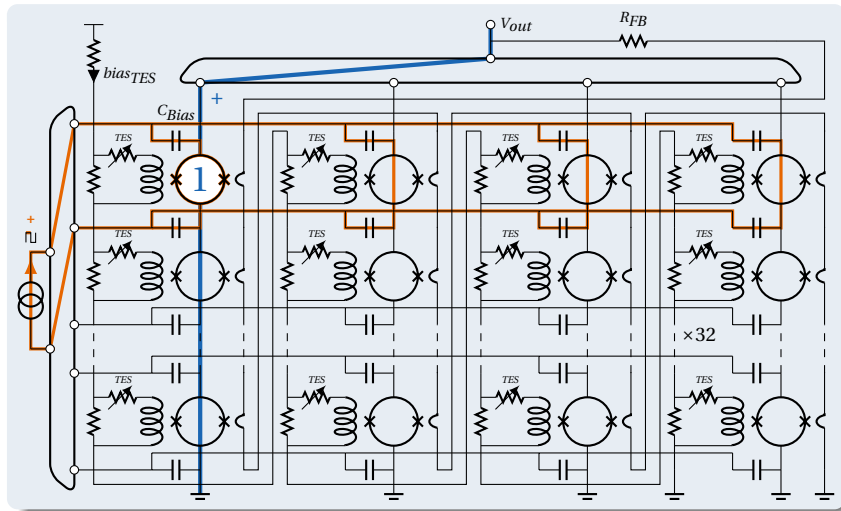
TES readout topology based on 2D multiplexing scheme



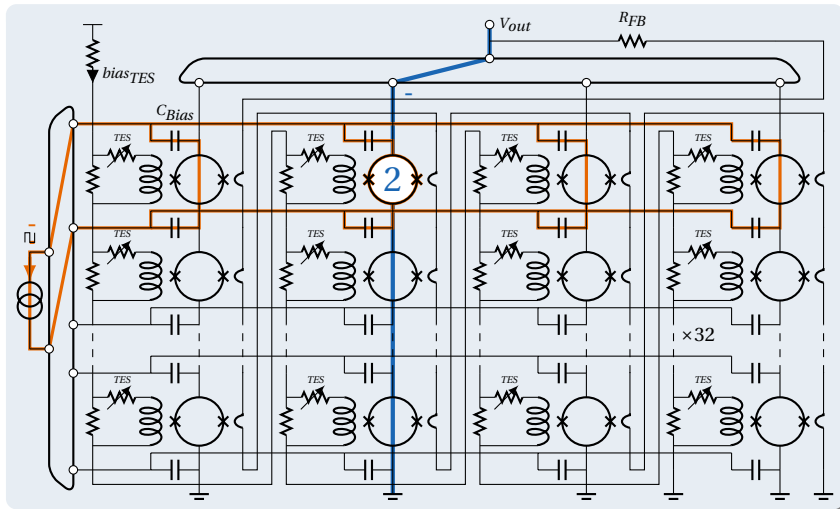
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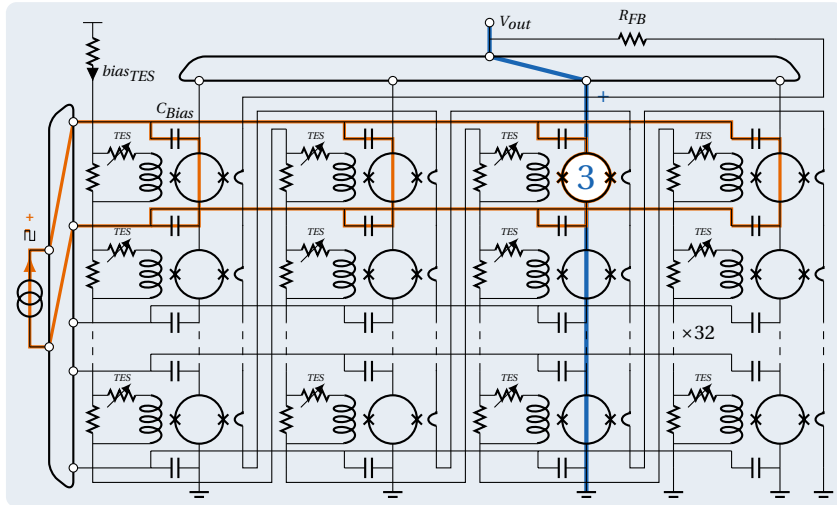
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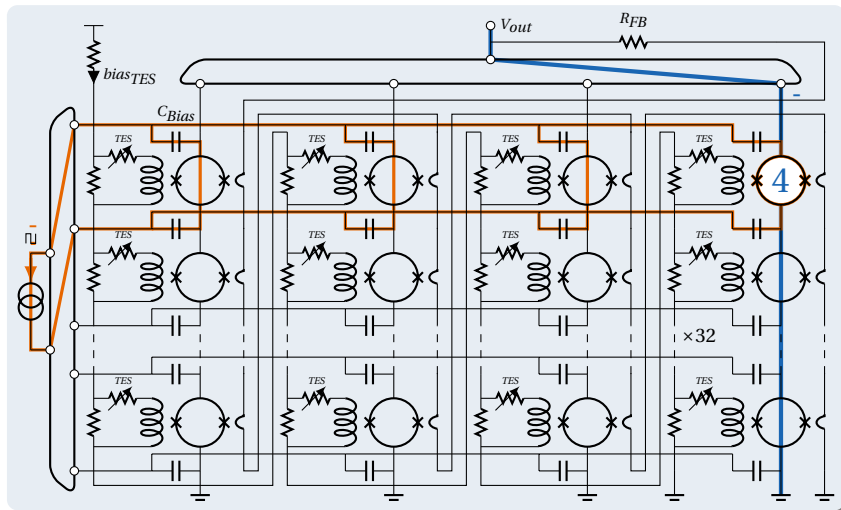
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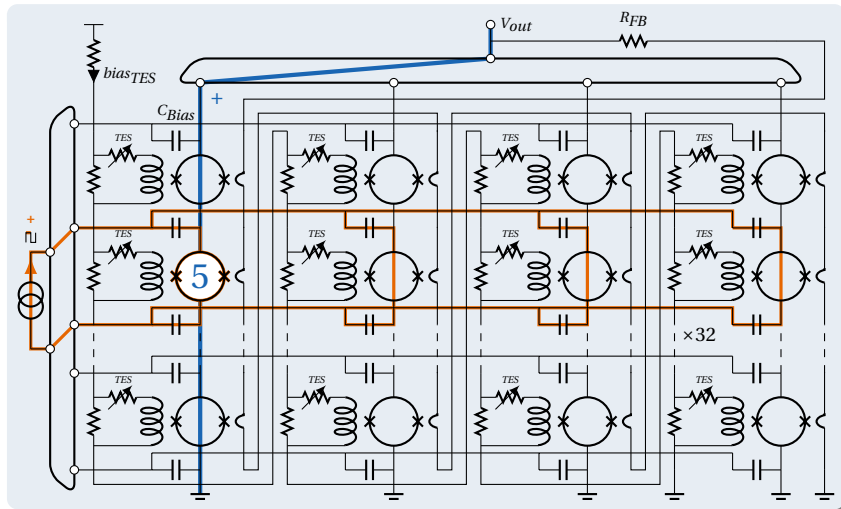
TES readout **topology** based on **2D** multiplexing scheme



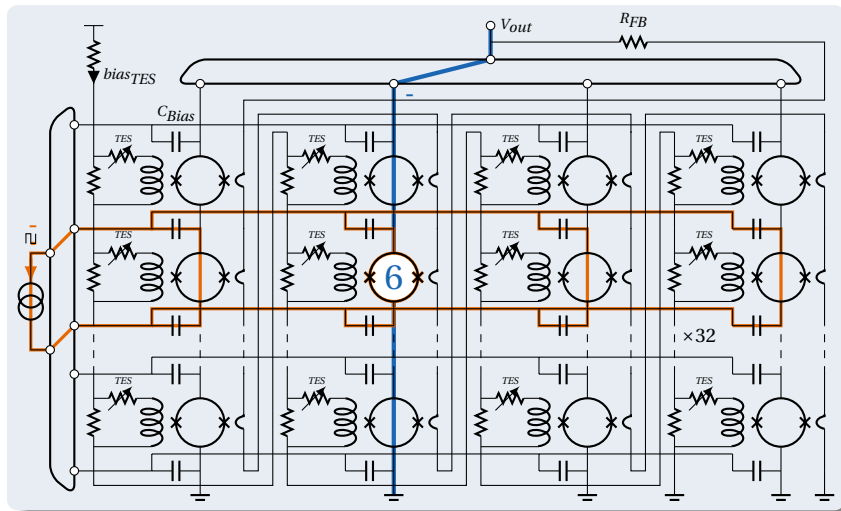
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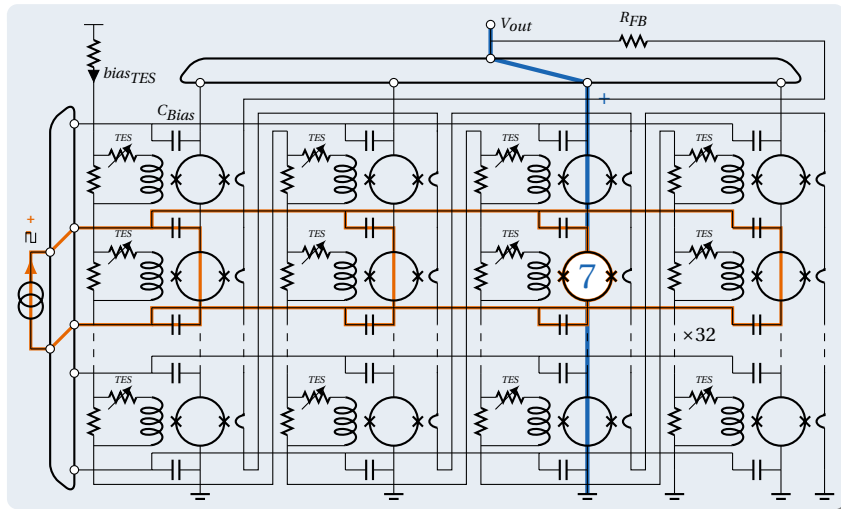
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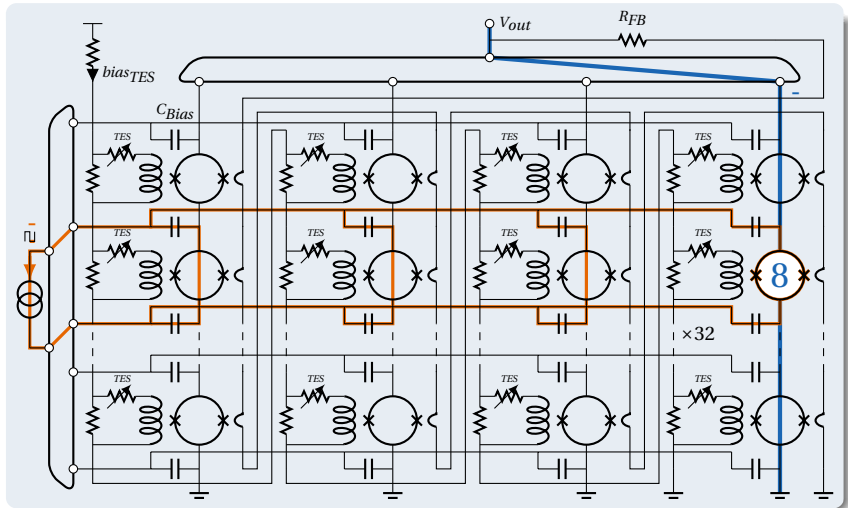
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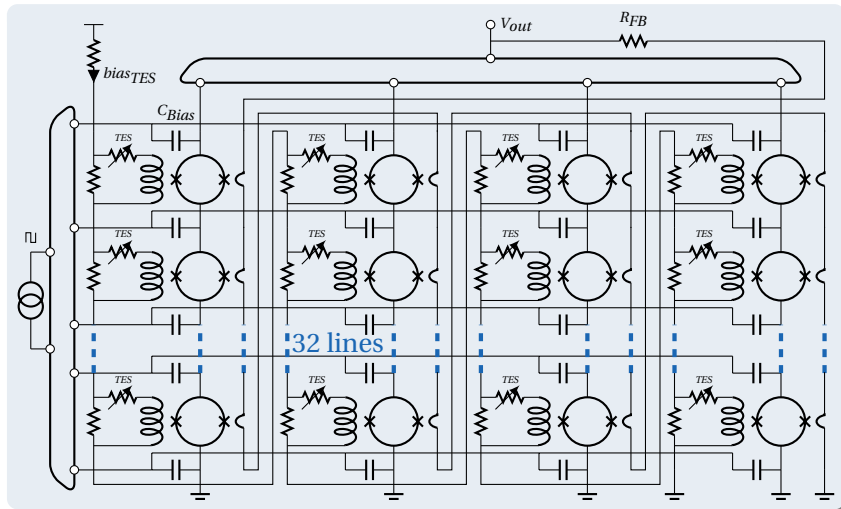
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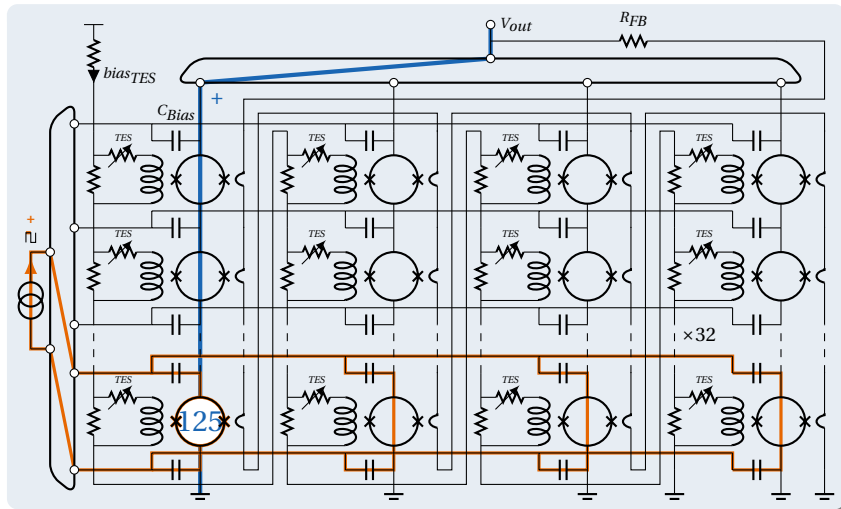
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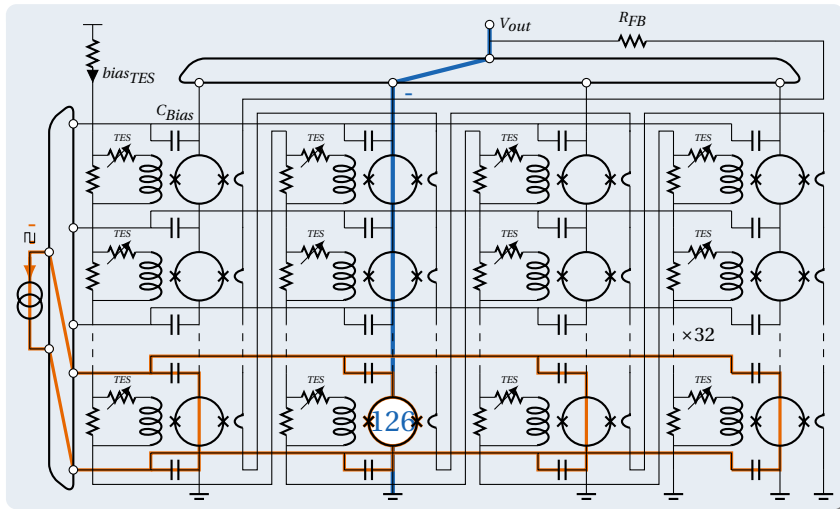
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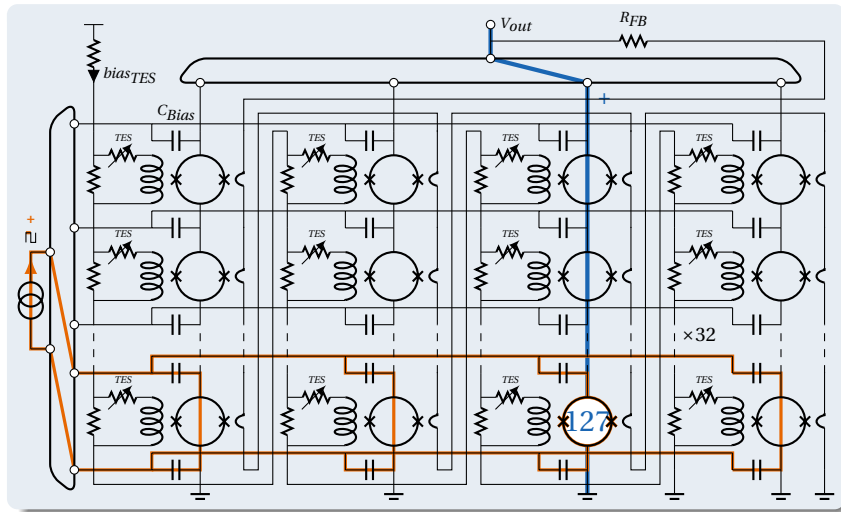
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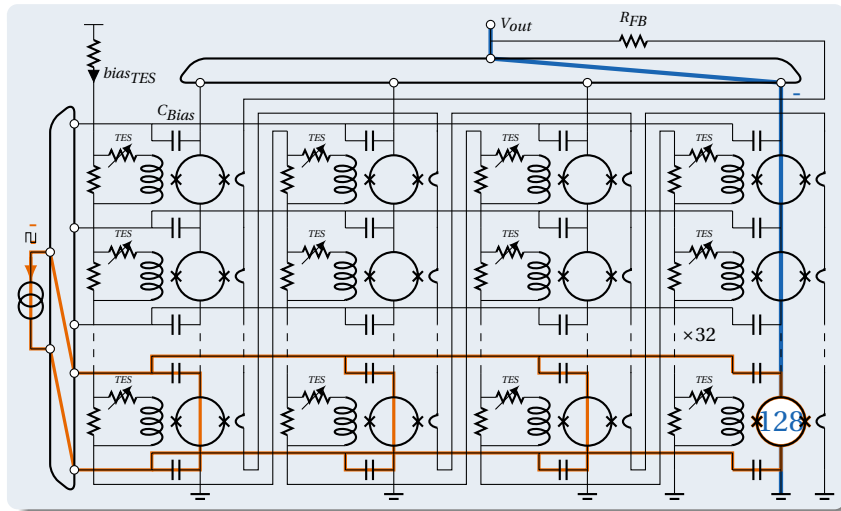
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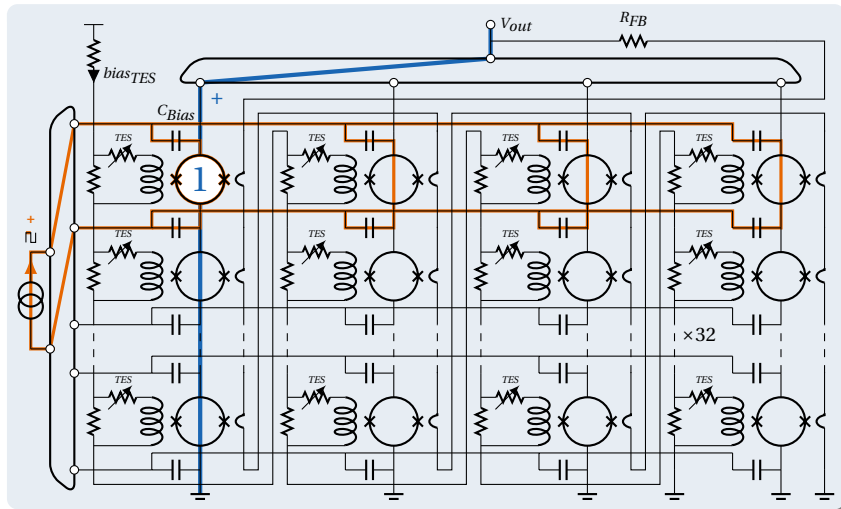
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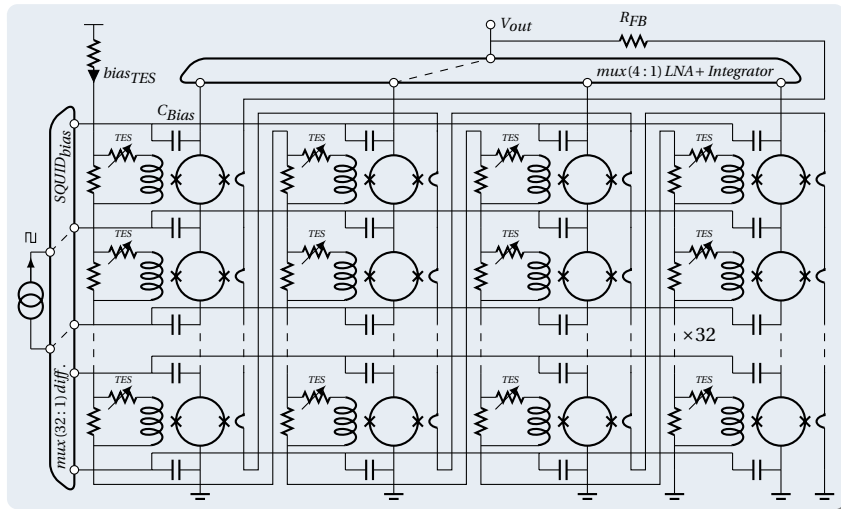
TES readout topology based on 2D multiplexing scheme



TES readout topology based on 2D multiplexing scheme



TES readout topology based on 2D multiplexing scheme



Outline

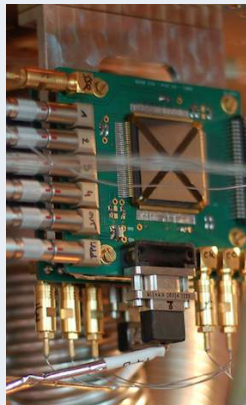
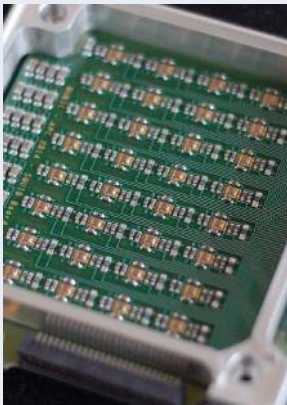
- 1 : 128 TDM multiplexer topology
- 2 Readout chain**
 - SQUID stage
 - Cryogenic integrated circuit
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Time domain SQUID multiplexer for QUBIC

QUBIC Readout sub-system : 256 TES, 256 SQUID, 2 ASIC

Sub-system : NbSi TES Wafer (300 mK) + 256 SQUIDs (1K) + 2 ASICs (40K)

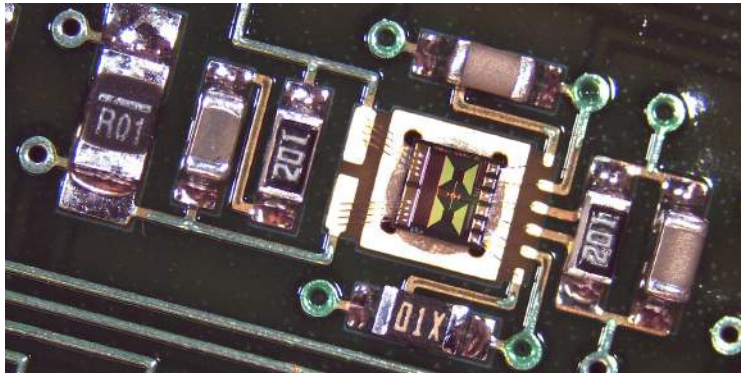


Integration of this sub-system in a dilution fridge for readout test



SQUID glued and wire bonded on a PCB

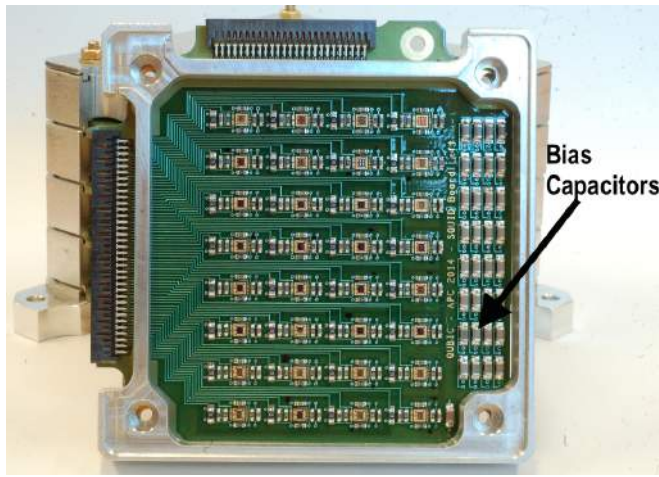
StarCryoelectronics SQ680 specific design.



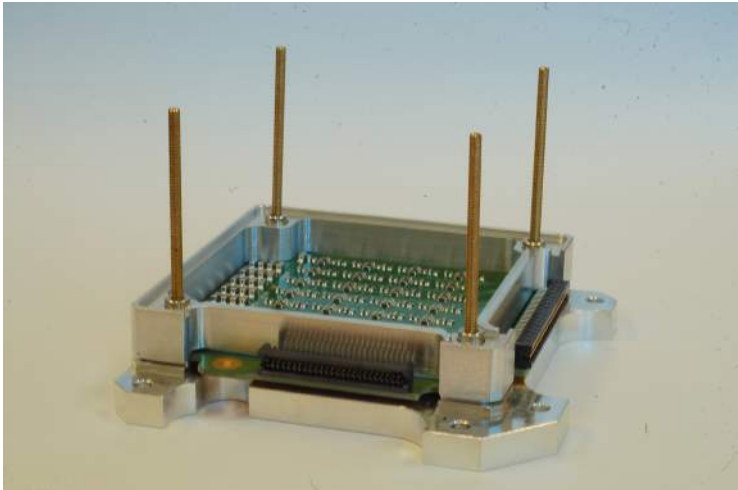
Solder plated track (no parasitic resistances)
Shunt resistor and filter devices



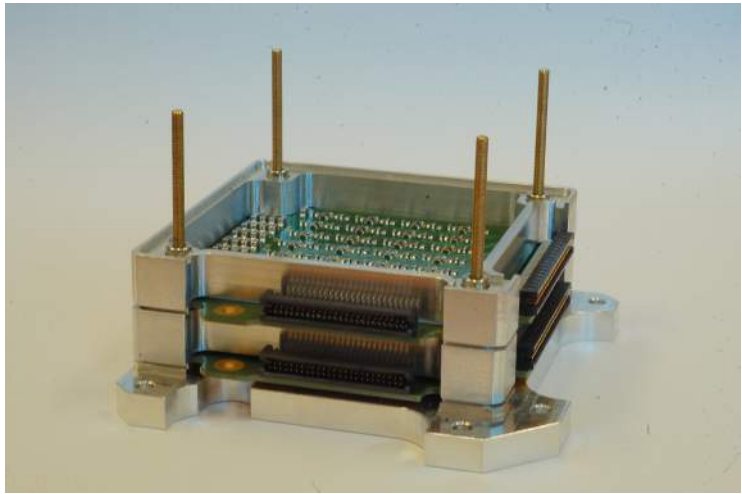
32 SQUIDs glued and wire bonded on a PCB



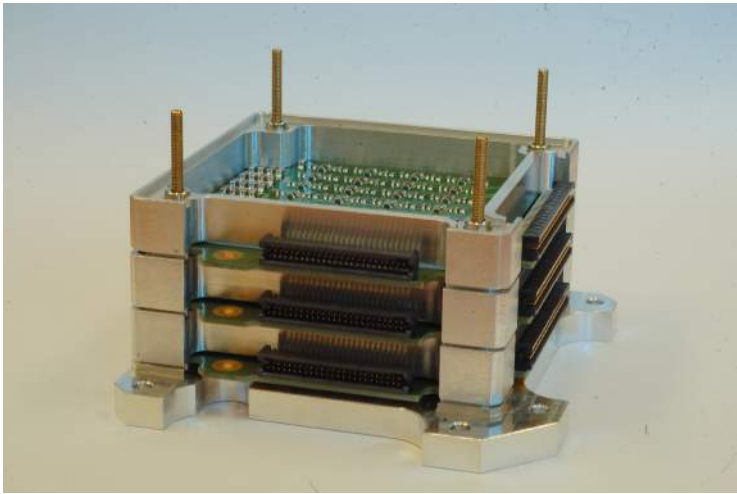
32 SQUIDs glued and wire bonded on a PCB



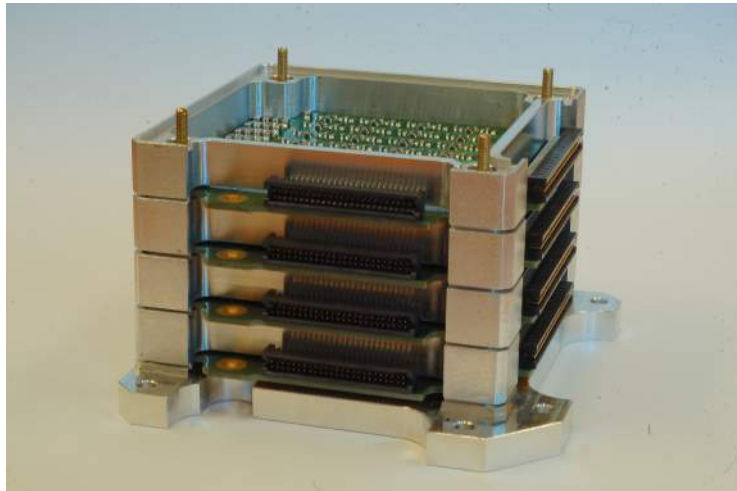
64 SQUIDs glued and wire bonded on a PCB



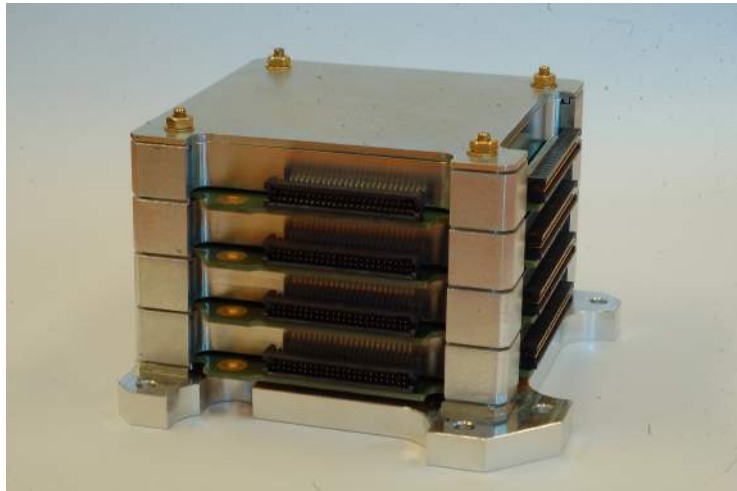
96 SQUIDs glued and wire bonded on a PCB



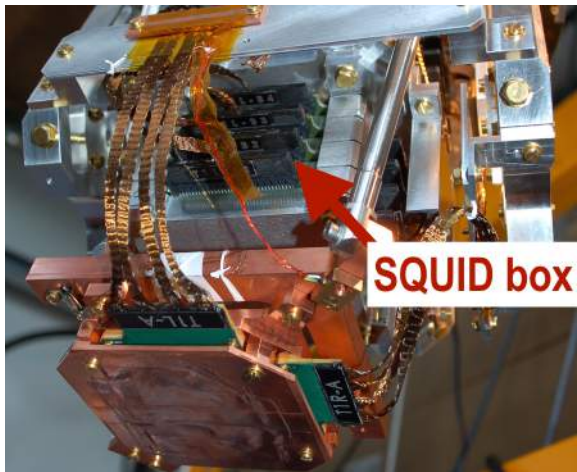
128 SQUIDs glued and wire bonded on a PCB



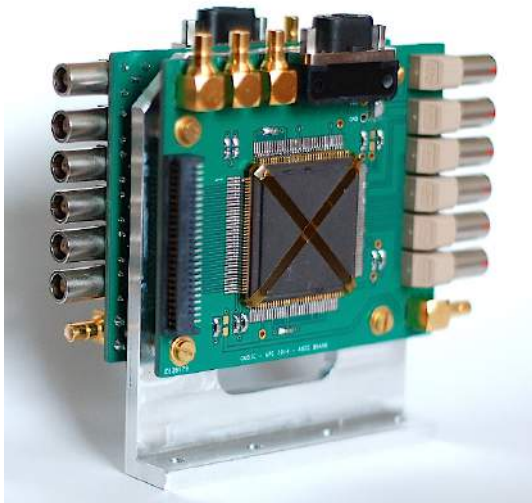
128 SQUIDs glued and wire bonded on a box



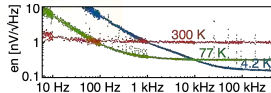
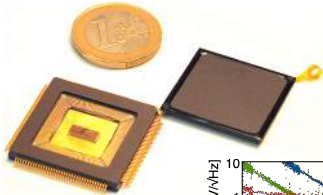
SQUIDs glued and wire bonded on a box



ASIC Stage (Application Specific Integrated Circuit)



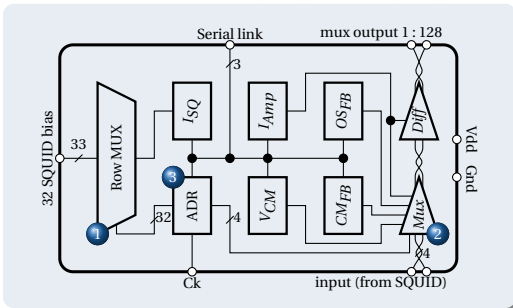
SiGe ASIC for cryogenic 1 : 128 TD SQUID M



BiCMOS SiGe ASIC

350nm AMS technology

- 1 SQUID rows addressing :
Biasing through capacitors with AC multiplexed current sources (1 : 32)
- 2 Low noise amplifier with multiplexed inputs :
FLL preamplifier
column mux. (1 : 4)
- 3 Digital addressing circuit controlled by external Ck



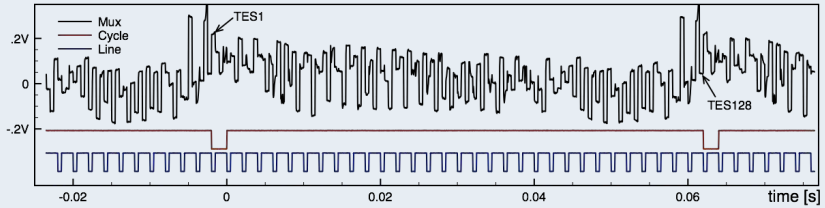
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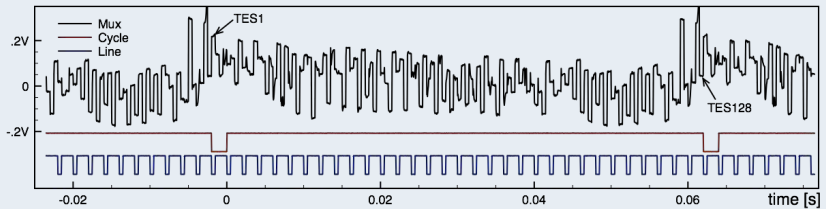
Multiplexed time line

1:128 multiplexing rate

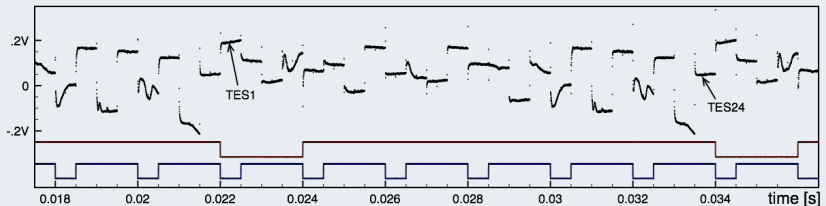


Multiplexed **time line**

1:128 multiplexing rate



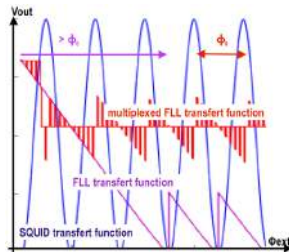
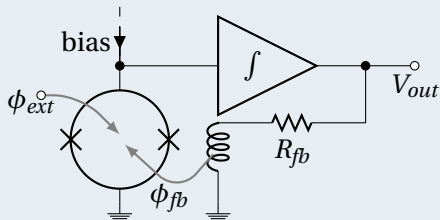
The ASIC allows to **reduce the part of the array readout**



Flux Locked Loop (FLL) in multiplexed mode

FLL to linearize the "sine-like" SQUID transfer function

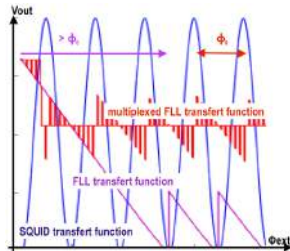
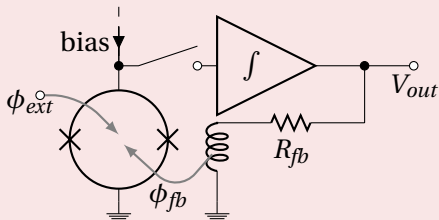
Analog FLL



Flux Locked Loop (FLL) in multiplexed mode

FLL to linearize the "sine-like" SQUID transfer function

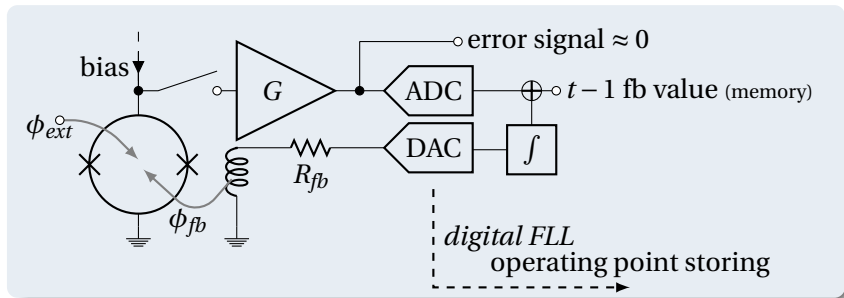
Multiplexed analog FLL



Multiplexed mode : FLL operating point jump a ϕ_0 between samples



"digital" FLL



Warm readout/acquisition (FPGA + ADC/DAC)

- Realtime feedback compensation implemented into the FPGA
- Series link with ASIC
- Power supply ASIC



IRAP collaboration



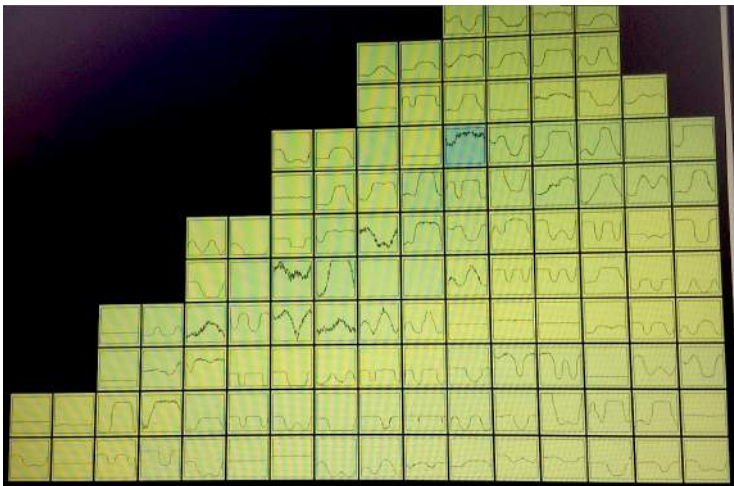
Demultiplexing software



IRAP collaboration



Demultiplexing software



IRAP collaboration



Conclusion and outlook

- Implementation and operation of a 1 : 128 TDM
- 2D multiplexing : SQUID stage + ASIC stage
- Demultiplexing and *digital FLL* in a FPGA

To be done soon :

- 1 Increase of multiplexing frequency
- 2 Noise measurements without aliasing

