High Speed Readout Electronics for Time and Code Division Multiplexing Applications: Critical Developments for Operation at 6.25 MHz Switching Rates

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Over two decades of effort at NIST has led to the realization of time and code division SQUID multiplexing systems capable of reading out TES microcalorimeter arrays of 100's of pixels. This has led to adoption of the technology for a variety of applications at facilities around the world. The results we will present concern the final developments required to attain the long sought ability to operate at switching rates of 6.25 MHz. These rates correspond to a dwell time per sensor of 160 ns and frame rates of 195 kHz for typical 32 row systems. Obstacles emerged during this work that were

specific to the desired switching rates. Examples include the performance limits of readily available semiconducting components and the intrinsic delays due to signal propagation within the multiplexing system. These obstacles have now been overcome.

We describe the modifications to hardware, firmware, and software that were required to attain the goal of 6.25 MHz switching rates. Major hardware challenges included; developing a PCIe based multichannel fiber optic receiver capable of sustained data rates of 1.6 Gbps, implementing compensation strategies for timing signal degradation on a backplane not optimized for these clock frequencies, and developing external trigger and synchronization circuitry to interface with other facility based systems. Firmware efforts we describe include; adopting encoding strategies to allow distributed high speed serial communications links between the crate and the data receiver, utilizing FPGA based dynamic phase reconfiguration at each signal transmitter to allow for phase calibration across the distributed system, realization of an arbitrary state sequencer capable of state switching in less then 16 ns, implementation of an auto relocking algorithm to mitigate flux jump events, and a pipelined digital feedback algorithm that distributes the cyclic logic latency over multiple states thereby reducing the overall switching time. Lastly, we discuss the completely redeveloped user interface necessary to accommodate the expanded functionality required to operate at these switching rates. Application examples and results will be shown to underscore the impact of this work.