Surface roughness effect on transition edge sensor microcalorimeters using multilayer readout wiring.

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This paper describes study of surface roughness effect on TES (Transition Edge Sensor) microcalorimeters using multilayer readout wiring. A large array of TES microcalorimeters has been developed for a future X-ray astronomy satellite DIOS (Diffuse Intergalactic Oxygen Surveyor) (Ohashi et al., 2014 SPIE). It aims at detection and mapping of warm hot intergalactic medium, which is expected to trace large-scale structure of the universe. For this purpose, the detector must cover a large effective area of 1 times 1 cm2 with the superb energy resolution of 2 eV in 0.3—1.5 keV.

We have fabricated TES arrays in-house and achieved energy resolution of 2.8 eV (FWHM) at 5.9 keV in a single pixel of a 8 times 8 array (Akamatsu et al., 2009 AICP) and 4.4 eV in a 16 times 16 pixel array (Ezoe et al., 2009 AICP). However, these arrays employ coplanar wiring, which can cause serious electrical crosstalk among closely-packed neighboring pixels. Hence, we are dedicating our efforts to develop multilayer readout wiring (Ezoe et al., 2013 IEEE TAS). Hot and return Al wiring sandwitching a insulation SiO2 layer are contacted via a contact hole as shown in the attached figure.

The thickness of the upper Al wiring, the lower wiring, and the SiO2 layer are 200 nm, 100nm, and 180 nm, respectively. Edges of the upper wiring are tapered to enhance electrical contact between the upper wiring and the TES layer. The TES layer consists of ~40 nm-thick Ti and ~110 nm-thick Au. With a test device comprising only upper wiring and TES, we confirmed proper super-normal transition around 100 mK with a residual resistance of 0.3 mΩ (Yamada et al., 2014 JLTP, Ezoe et al., 2015 IEEE TAS).

We then proceeded to fabricate a 20 times 20 array of TES microcalorimeters on the multilayer wiring consisting of both upper and lower wires. However, none of our samples showed proper super-normal transition. In order to examine its cause, we investigated surface roughness effect of the bottom layers: i.e., the lower wiring and the insulation layer. We found that the surface roughness of the lower Al wiring coated with sputtering is large, ~3 nm rms at 1 micrometer scale, while that of the insulation layer deposited with liquid source chemical vapor deposition is ~0.2 nm. Furthermore, the TES film coated on the insulation layer showed a sharp transition at 170 mK with a residual resistance of ~2.5 mΩ, while that on both the lower Al wiring and the insulation layer did not show a transition. Hence, we presume that the surface roughness influences the transition properties. To avoid the surface roughness effect, we are testing two mitigations: (1) the lower Al wiring bypassing beneath the TES layer, and (2) smoothing the Al layer. In this paper, we will show results of these improvements.